ANALOG & DIGITAL ELECTRONICS

Laboratory Manual

Department of Electrical and Electronics Engineering

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(Autonomous Institution under JNTU Hyderabad)

Analog and Digital Electronics Lab Record

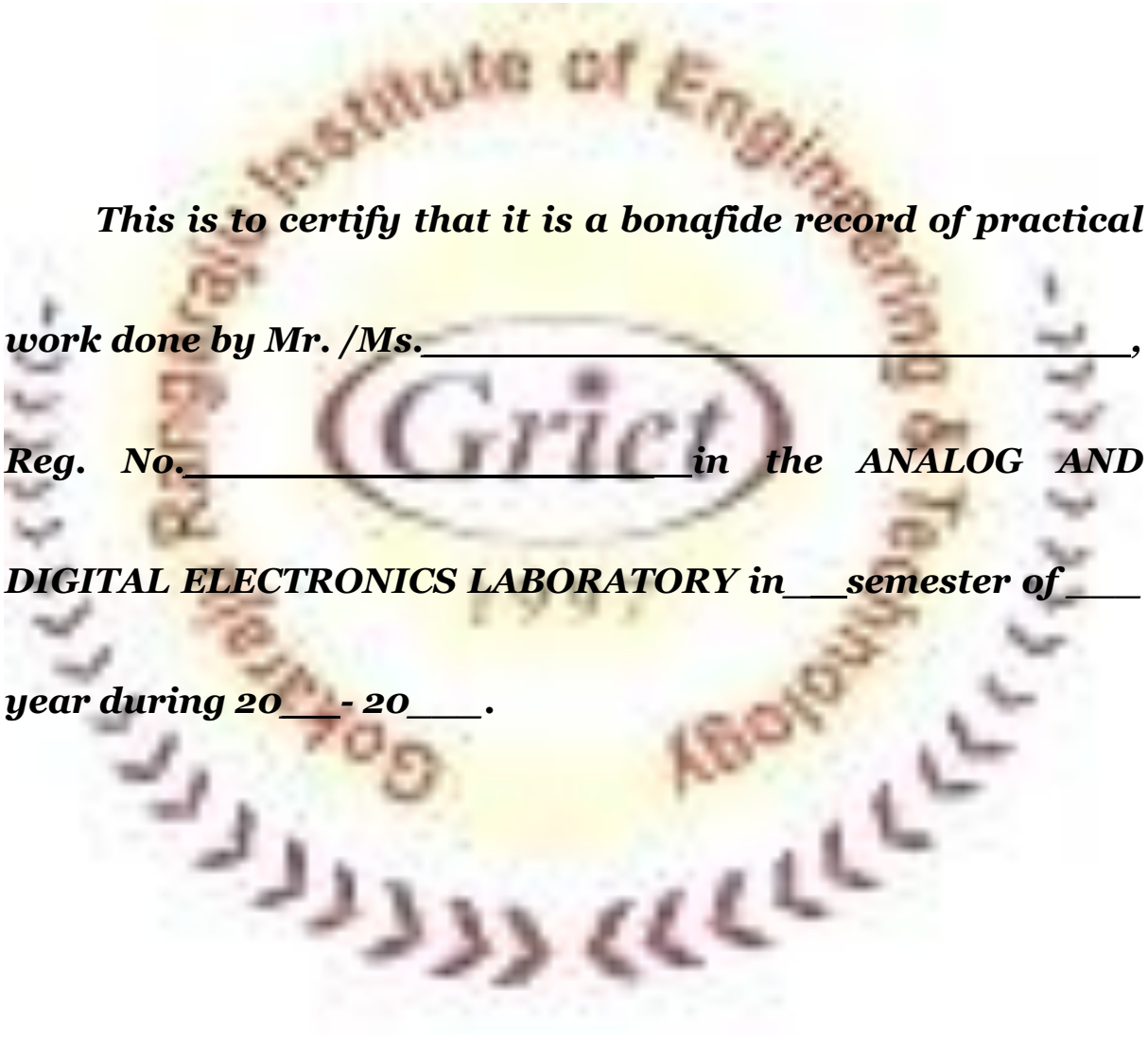
Name:

Reg no.:

Course: B.Tech.____ Yr____Semester

Branch: EEE

CERTIFICATE



This is to certify that it is a bonafide record of practical work done by Mr. /Ms._____, Reg. No._____in the ANALOG AND DIGITAL ELECTRONICS LABORATORY in___semester of____ year during 20___- 20____.

Internal Examiner
Signature

External Examiner
Signature

CONTENTS

INTRODUCTION TO ANALOG DISCOVERY KIT

Overview

The Digilent make "Analog Discovery Kit" is made in conjunction with Analog Devices, it is a multi- function instrument that can measure, record and generate analog and digital signals.

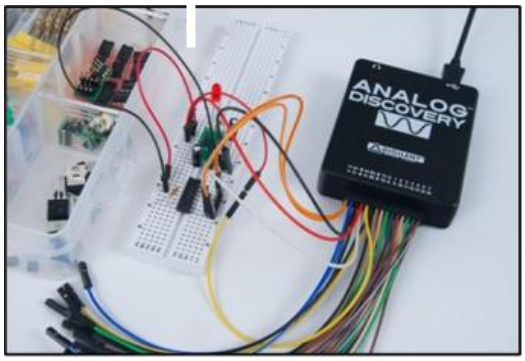


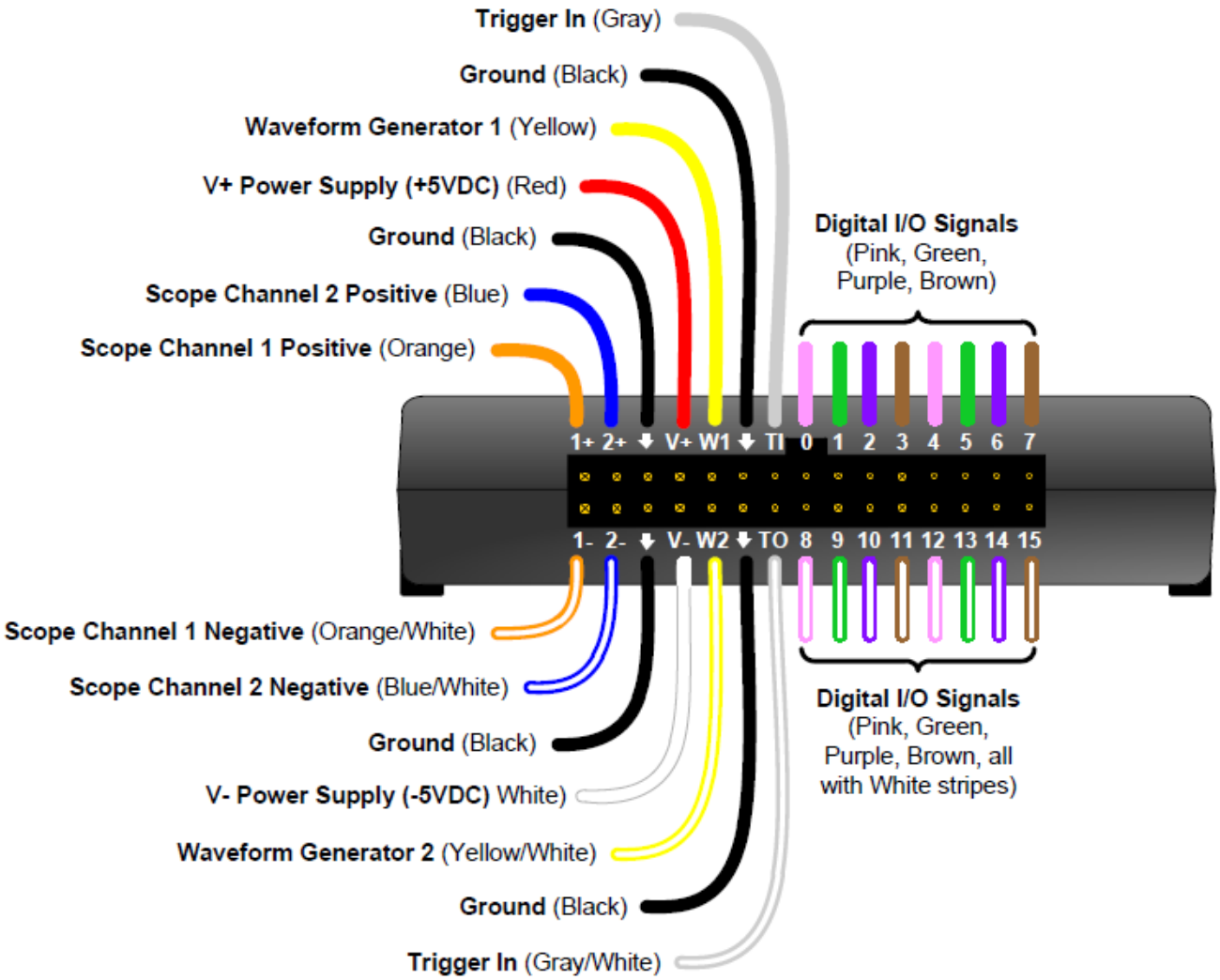
Figure: Analog Discovery used in a circuit design experiment

The small, portable and low-cost Analog Discovery (above Figure) was created so that engineering students could work with analog and digital circuits anytime, anywhere - right from their PC. The Analog Discovery's analog and digital inputs and outputs connect to a circuit using simple wire probes. Inputs and outputs are controlled using the free PC- based Waveforms software that can configure the Discovery to work as any one of several traditional instruments. Instruments include:

- Two channel oscilloscope (1MΩ, ±25V, differential, 14 bit, 100Msample/sec, 5MHz bandwidth);
- Two channel arbitrary function generator (22Ω, ±5V, 14 bit, 100Msample/sec, 5MHz bandwidth);
- Stereo audio amplifier to drive external headphones or speakers with replicated AWG signals;
- 16-channel digital logic analyzer (3.3V CMOS, 100Msample/sec)*;
- 16-channel pattern generator (3.3V CMOS, 100Msample/sec)*;
- 16-channel virtual digital I/O including buttons, switches and LEDs –good for logic trainer applications*;
- Two input/output digital trigger signals for linking multiple instruments (3.3V CMOS);
- Two power supplies (+5V at 50mA, -5V at 50mA).
- Single channel voltmeter (AC, DC, ±25V);
- Network analyzer – Bode, Nyquist, Nichols transfer diagrams of a circuit. Range: 1Hz to 10MHz;
- Spectrum Analyzer - power spectrum and spectral measurements (noise floor, SFDR, SNR, THD, etc.);
- Digital Bus Analyzers (SPI, I2C, UART, Parallel);

The Analog Discovery was designed for students in typical university-based circuits and electronics classes. Its features and specifications, including operating from USB power, a small and portable form factor, and the ability to be used by students in a variety of environments at low cost, are based directly on inputs from many professors at many universities. Meeting all the requirements proved challenging, and resulted in some new and innovative circuits. This document is a reference for the Analog Discovery's electrical functions and operations. This reference also provides a description of the hardware's features and limitations. It is not intended to provide enough information to enable complete duplication of the Analog Discovery, or to allow users to design custom configurations for programmable parts in the design.

The pin-out terminals of Analog Discovery Kit(AD Kit) is shown below



STEPS TO RUN WAVEFORM SOFTWARE

Step1: Open the "Waveform" software from the start menu of the windows desktop

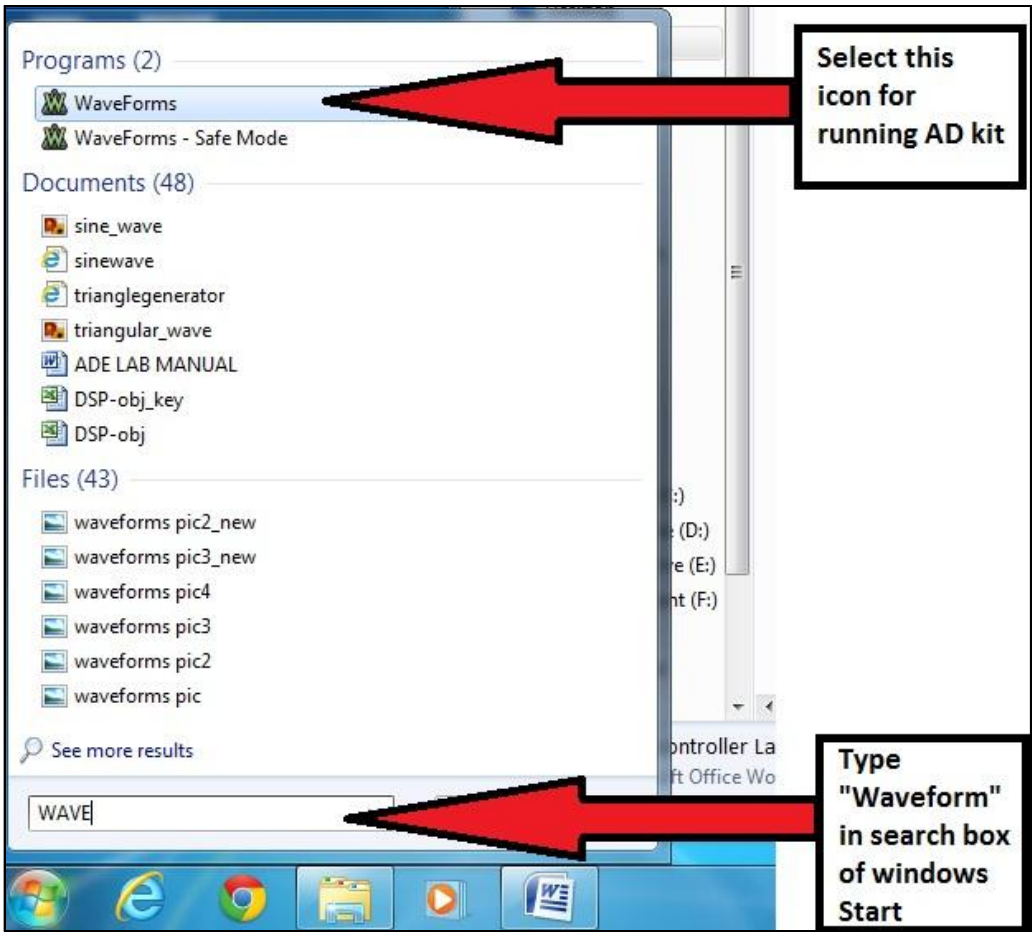


Figure: Showing the selection of Waveform software from the start menu

Step2: Each block representation of Waveform software

"in" -To check waveforms at the output terminals of the hardware connections done on Bread board "in" is selected

"out"- To give different input signals to the circuit done on the Bread board "out" is selected

"voltage"-This option is selected to apply +Vcc and –Vcc to the circuit connections done on Bread board

Figure: showing the Window of Waveform software

Step 3: The window shown below is obtained when "in" is selected from the "Waveform" software. Two waveforms can be seen at one time (one is "orange" and the other is "Blue"). The right side window shows the settings of different waveforms who's Y and X axis can be set. After selecting the required options, click the "Run" button on Top left side of the Window to see the obtained output of the circuit connected on the Bread board.

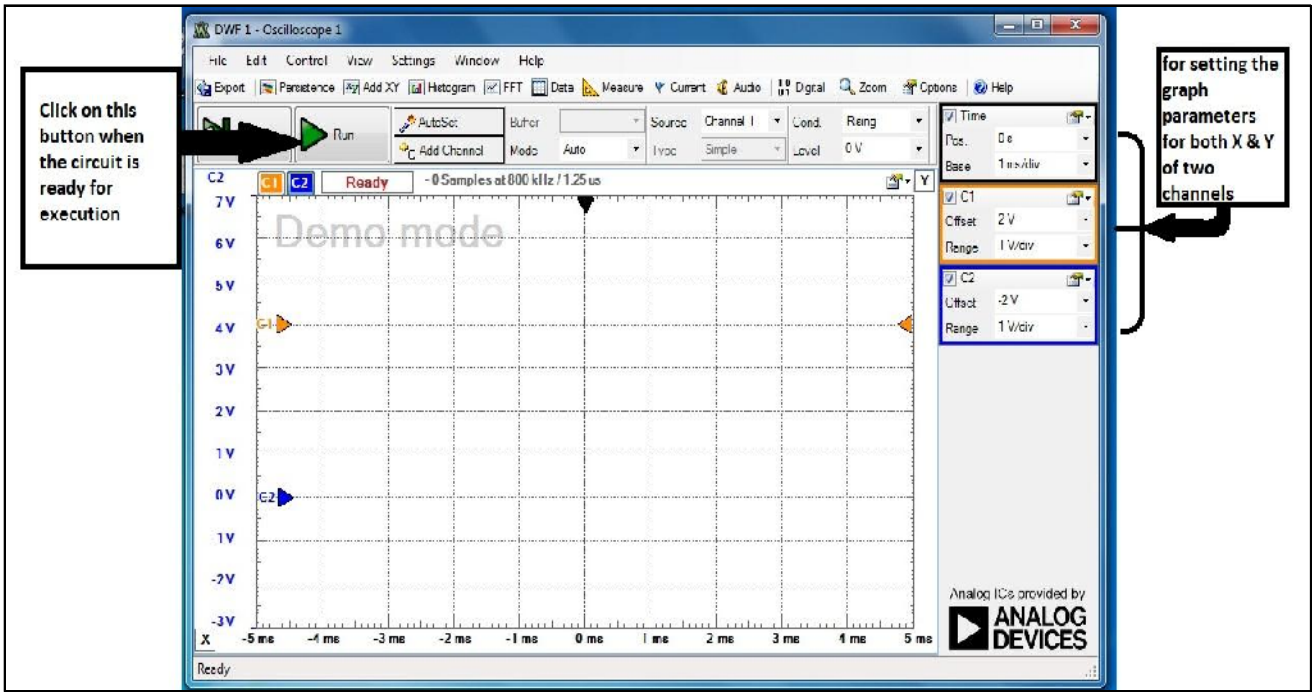


Figure: Shows the "in" window of "Waveform" software

Step4: "Out" tab of Waveform software is used for selecting the types of waveforms like-sinusoidal, square, triangular, trapezoidal, random signal of different frequencies from this window. The signal selected from this window is given as input signal to the circuit connected on

the Bread board. After making the required settings click on the "Run AWG1" option from the window.

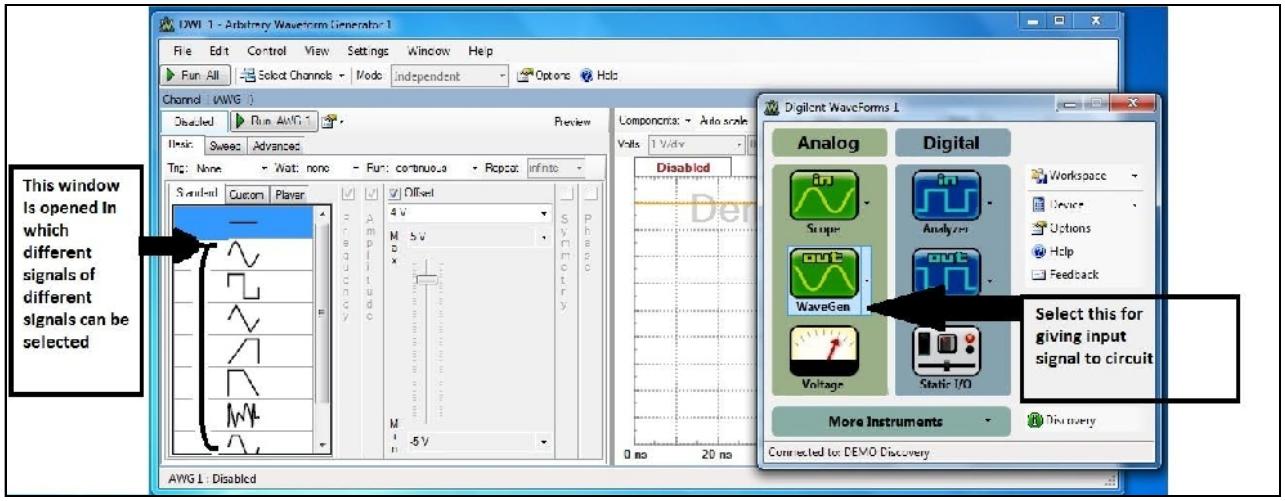


Figure: The "Out" window of Waveform in which different waveforms can be given as input

Step5: "Voltage" is selected for giving the input voltage of either +Vcc (Constant +5V) or –Vcc (Constant -5V) or both. When the "Power is ON/OFF" is selected the respective voltages are applied to the circuit connected.

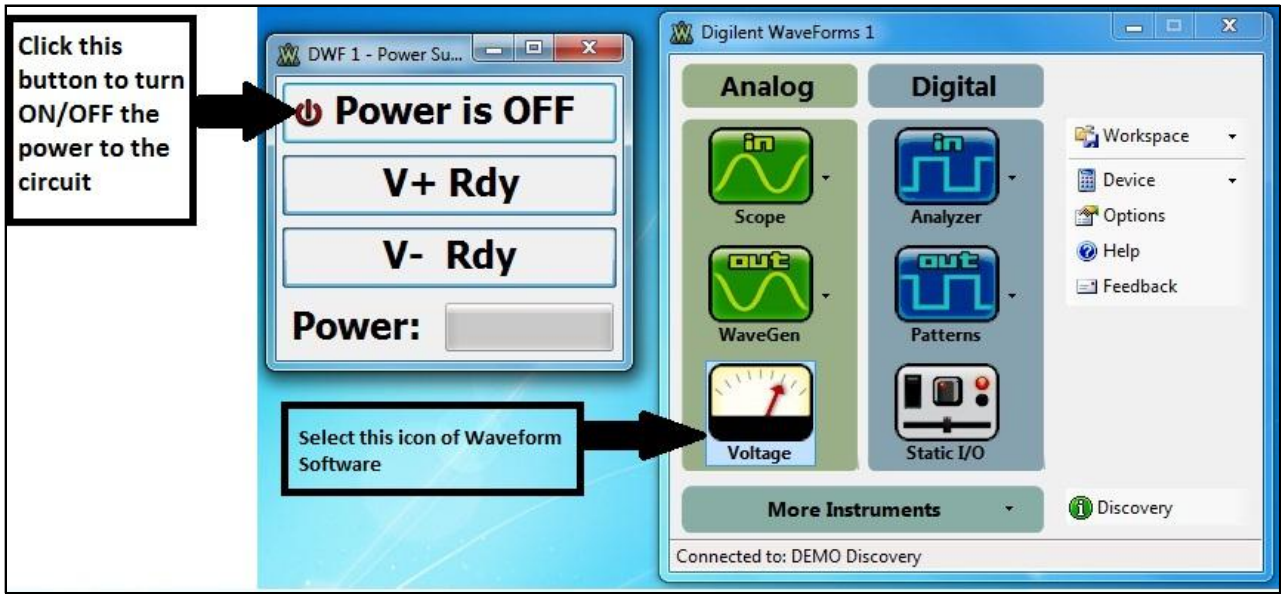


Figure: The "Voltage" window of Waveform helps to run the ADE kit

EXPERIMENT-1

PROPORTIONAL AMPLIFIER

AIM: To demonstrate Proportional Amplifier Circuit using Op-Amp.

APPARATUS: 741/OP27 IC or its equivalent

1KΩ Resistors

Analog Discovery Kit (AD Kit), Connecting Wires

Breadboard

CIRCUIT DIAGRAM:

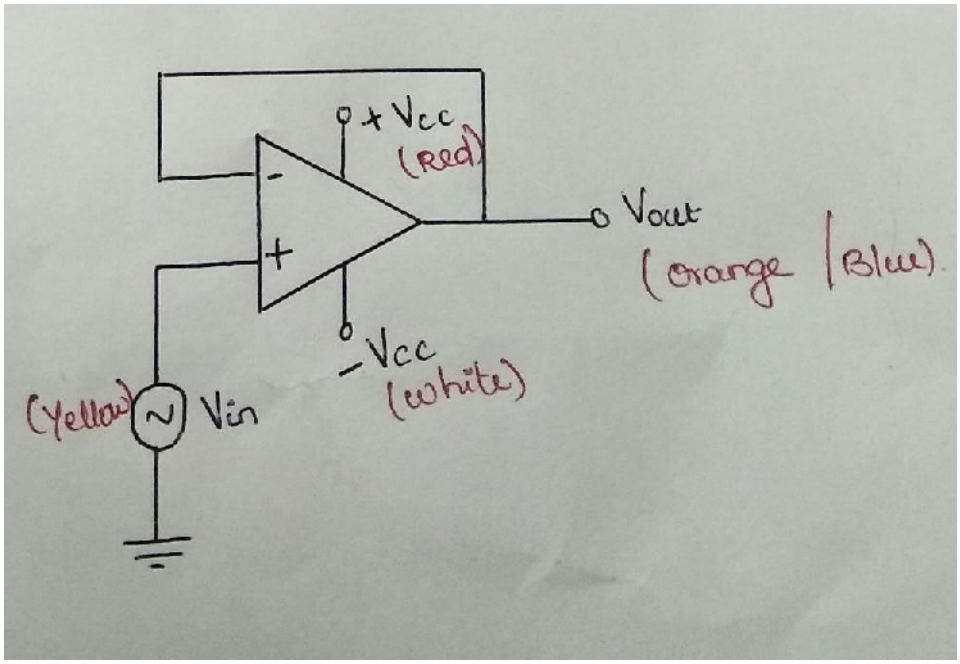


Figure: Proportional Ampilifier

PROCEDURE:

1. Connect the components as per the circuit diagram on the Bread board
2. Adjust the input voltage starting with DC 500mv and find the output voltage.
3. Find the Output Voltage for values mentioned in the table and note down the values.
4. Repeat the same with for different values of input sine waveform also and note down the values on the table.

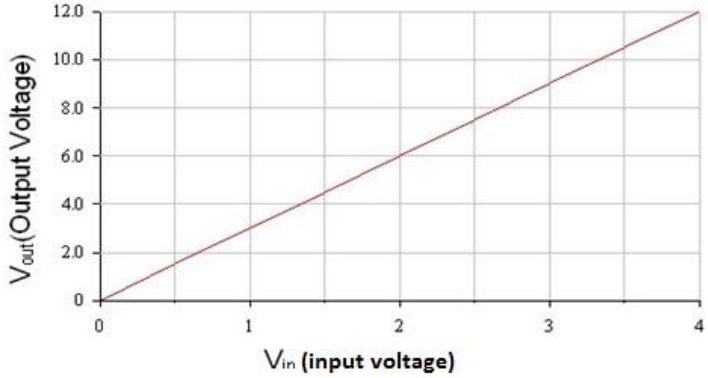
Tabular Column for DC input voltage:

S. No	V_{in}	V_{out}	V_{out}/V_{in}
1	500mV		
2	1.5mV		
3	2mV		

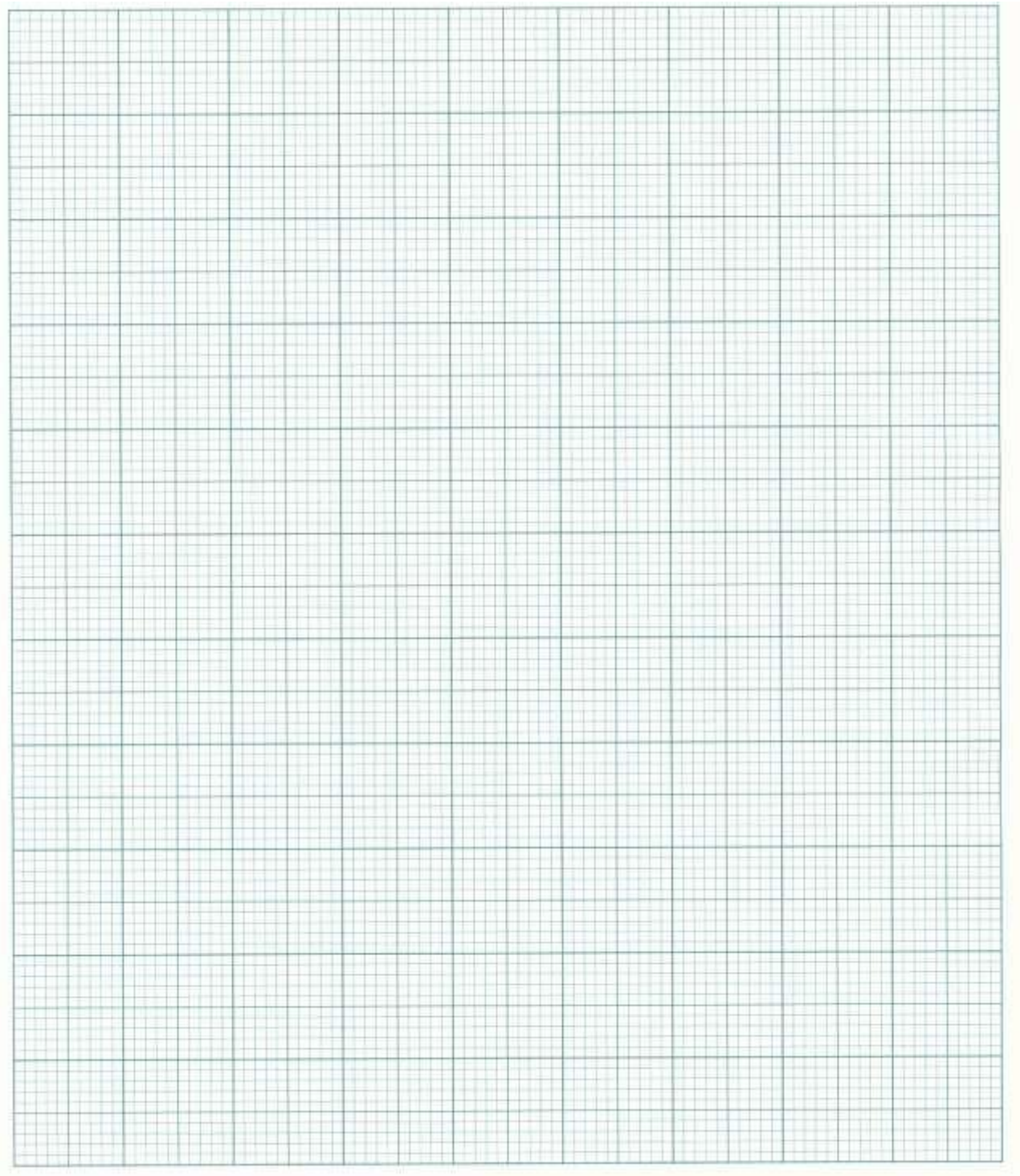
Tabular Column for AC (Sine Wave) input voltage:

S. No	V_{in}	V_{out}	V_{out}/V_{in}
1	500mV		
2	1.5mV		
3	2mV		

MODEL GRAPH:



GRAPH SHEET:



RESULT:

EXPERIMENT-2

INVERTING AMPLIFIER

AIM: To demonstrate Inverting Amplifier Circuit using Op-Amp.

APPARATUS: 741/OP27 IC or its equivalent

10 KΩ, 1KΩ Resistors

Analog Discovery Kit (AD Kit), Connecting wires

Breadboard

CIRCUIT DIAGRAM:

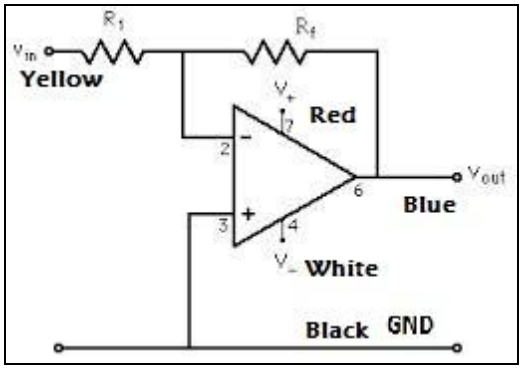


Figure: Inverting Amplifier

THEORY:

As the open loop DC gain of an Operational Amplifiers is extremely high we can therefore afford to lose some of this high gain by connecting a suitable resistor across the amplifier from the output terminal back to the inverting input terminal to both reduce and control the overall gain of the amplifier. This then produces and effect known commonly as Negative Feedback, and thus produces a very stable Operational Amplifier based system.

Negative Feedback is the process of "feeding back" a fraction of the output signal back to the input, but to make the feedback negative, we must feed it back to the negative or "inverting input" terminal of the op-amp using an external Feedback Resistor called Rf. This feedback connection between the output and the inverting input terminal forces the differential input voltage towards zero.

This effect produces a closed loop circuit to the amplifier resulting in the gain of the amplifier now being called its Closed-loop Gain. Then a closed-loop inverting amplifier uses negative feedback to accurately control the overall gain of the amplifier, but at a cost in the reduction of the amplifiers gain. This negative feedback results in the inverting input terminal having a different signal on it than the actual input voltage as it will be the sum of the input voltage plus the negative feedback voltage

giving it the label or term of a *Summing Point*. We must therefore separate the real input signal from the inverting input by using an Input Resistor, Rin.

In this Inverting Amplifier circuit the operational amplifier is connected with feedback to produce a closed loop operation. When dealing with operational amplifiers there are two very important rules to remember about inverting amplifiers, these are: "No current flows into the input terminal"and that "V1 always equals V2". However, in real world op-amp circuits both of these rules are slightly broken.

This is because the junction of the input and feedback signal (X) is at the same potential as the positive (+) input which is at zero volts or ground then, the junction is a "Virtual Earth". Because of this virtual earth node the input resistance of the amplifier is equal to the value of the input resistor, Rin and the closed loop gain of the inverting amplifier can be set by the ratio of the two external resistors.

$$Vout = -\frac{Rf}{Rin} \times Vin$$

We said above that there are two very important rules to remember about Inverting Amplifiers or any operational amplifier for that matter and these are.

1. No Current Flows into the Input Terminals
2. The Differential Input Voltage is Zero as V1 = V2 = 0 (Virtual Earth)

PROCEDURE:

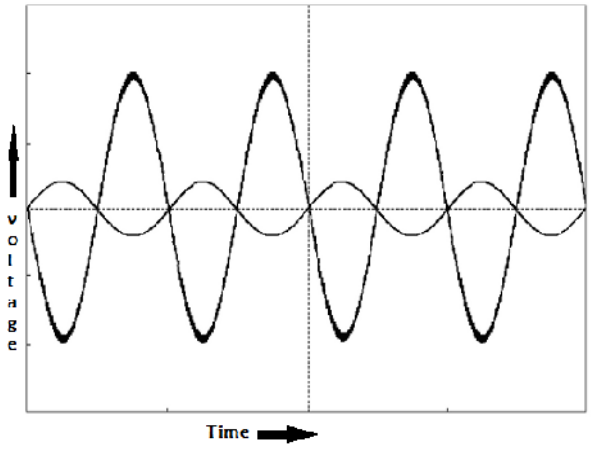
1. Connect the components as per the circuit diagram on the Bread board
2. The color terminals represent the connections made with respect to the Analog Discovery kit at the respective terminals on the Bread board
3. Adjust the input voltage starting with 500mv and find the output voltage.
4. Repeat the above steps for different voltages by taking different input signals
5. Draw the graph between input and output voltages for the values obtained from the table.

Tabular Column:

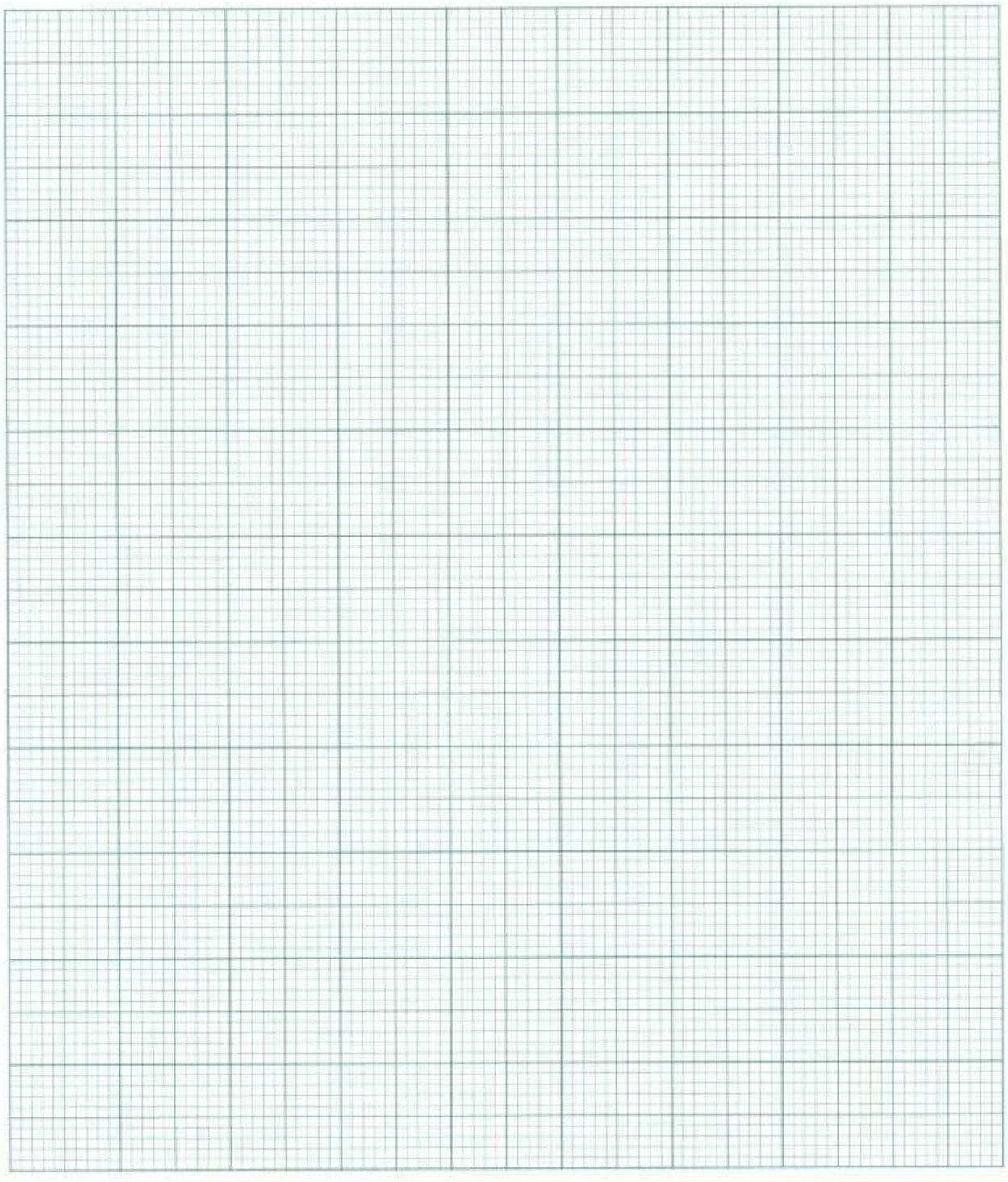
S. No	V_{in}	V_{out}	V_{out}/V_{in}

THEORETICAL CALCULATIONS:

MODEL GRAPH:



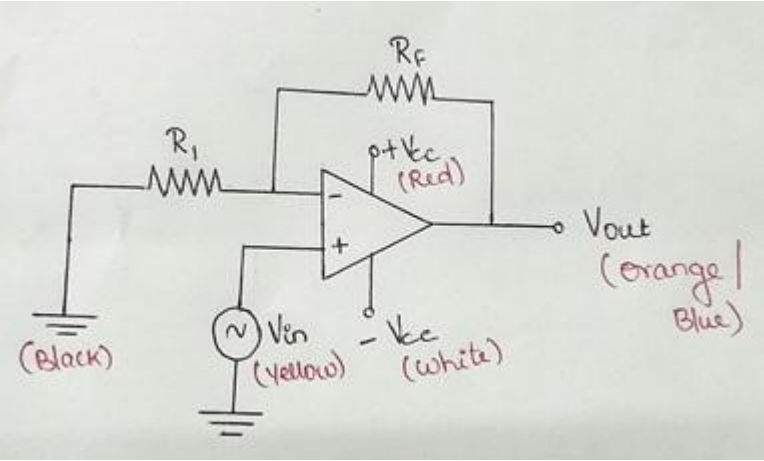
GRAPH SHEET:



RESULT:

Exercise:

1. Execute the following "Non inverting Amplifier" circuit with different values of Rf resistance



EXPERIMENT-3

INTEGRATOR

AIM: To demonstrate Integrator Circuit using Op-Amp

APPARATUS: 741/OP27 IC or its equivalent

10 KΩ, 1KΩ Resistor

100nF Capacitor

Analog Discovery Kit (AD Kit), Connecting Wires

Breadboard

CIRCUIT DIAGRAM

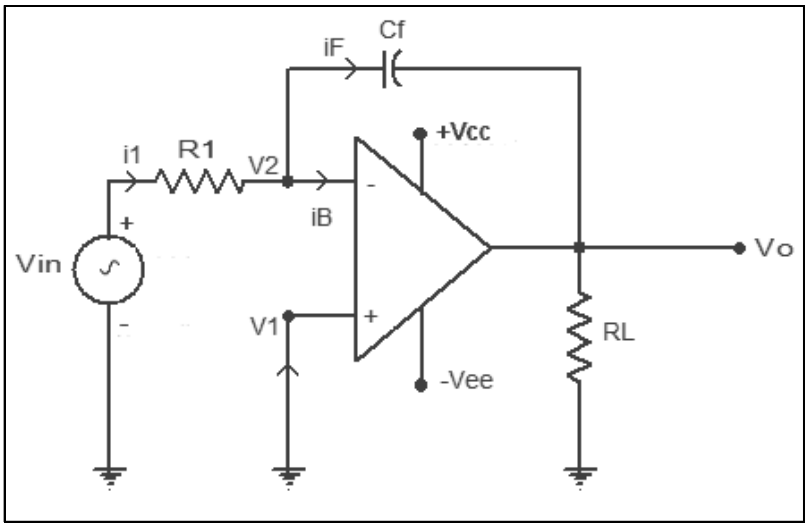


Figure: Integrator

THEORY:

It is a low pass RC filter circuit. It can work as an integrator when time constant is very large. This requires very large values of R and C by Miller's theorem the effective input capacitance becomes C!(1-Av)where Av is the gain of the op-amp. The gain Av is infinite for an ideal op-amp.so, the effective time constant of the op-amp becomes large which results in perfect integration. The output voltage of an integrator is shown below

$$Vo = \frac{-1}{R1\ Cf} \int_{o}^{t} Vin\ dt + C$$

PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Suitable R_f and $C_{1\ are}$ chosen such that the output of the circuit is the integral of the input voltage.
3. Apply square wave or sine wave input voltage (V) or any other type of signal at the input terminal.
4. Observe the output voltage waveform on the CRO and note down the corresponding values.
6. The time constant R_fC_1 is changed by changing the values of R_f or C_1 and the corresponding output waveforms are noted.

MODEL GRAPHS:

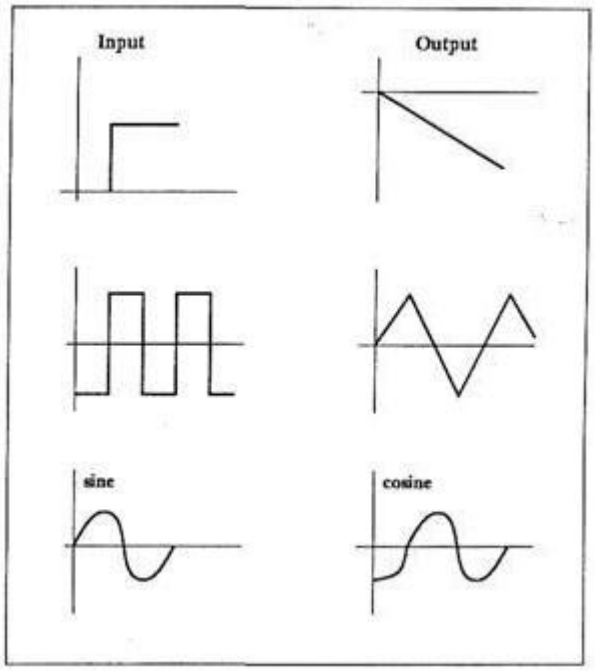


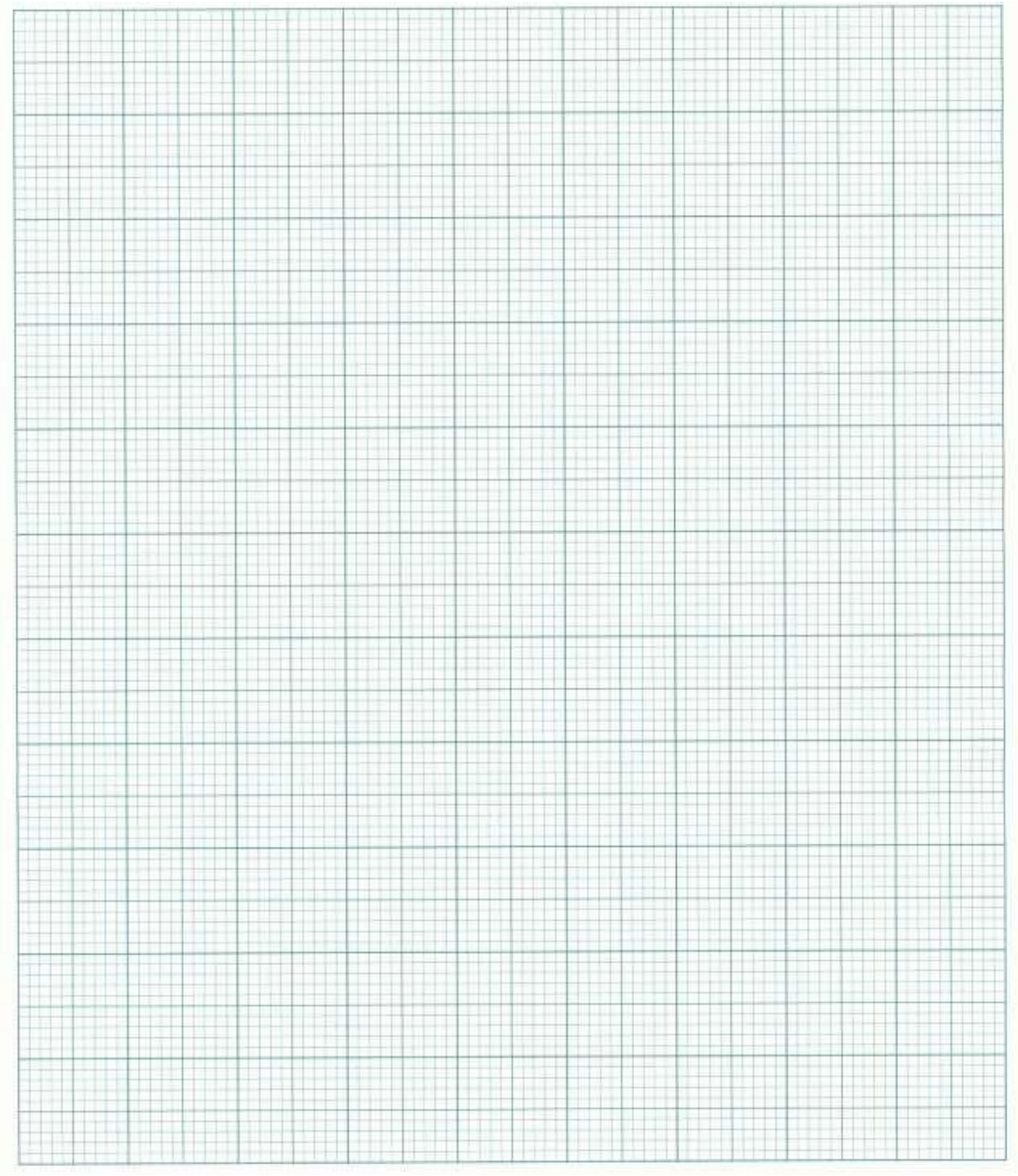
Figure: Model Graphs for Integrator

Tabular Column

S. No	V_{in}	V_{out}	V_{out}/V_{in}

Theoretical Calculations:

GRAPH SHEET:



RESULT:

EXPERIMENT-4

DIFFERENTIATING AMPLIFIER

AIM: To demonstrate Differentiate Amplifier Circuit using Op-Amp.

APPARATUS: 741/OP27 IC or its equivalent (1)

10 KΩ, 1.5KΩ Resistors

0.1µF Capacitor

Analog Discovery Kit (AD Kit), Connecting Wires

Breadboard/PCB

CIRCUIT DIAGRAM:

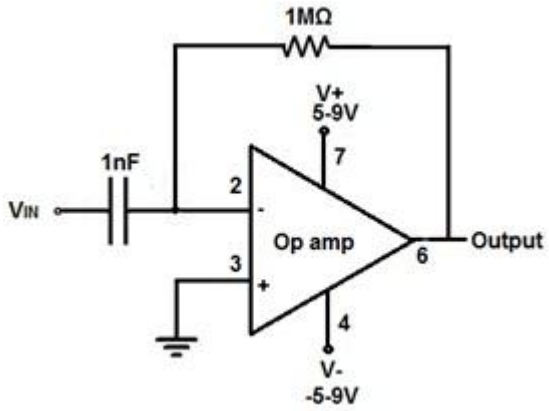


Figure: Differentiator

THEORY:

It consists of an high pass RC filter .it acts as a differentiator for low values of time constant. Here the output is the derivative of the input signal by

Thus output is not only the derivative of the input but also out of phase by 180^o with respect to the input.

$$V_{out} = -RC\frac{dV_{in}}{dt}$$

Here $R_2=R$ and $C_1=C$

PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Suitable values of R_1, R_2, C_1, C_2 are chosen such that the output of the circuit is the integral of the input voltage.
3. A square wave input voltage (V) is applied at the input terminal.
4. Observe the output voltage waveform on the CRO and note down the corresponding values.
5. The time constant R_2C_1 is changed by changing the values of R_2 or C_1 and the corresponding output waveforms are noted.

MODEL GRAPHS:

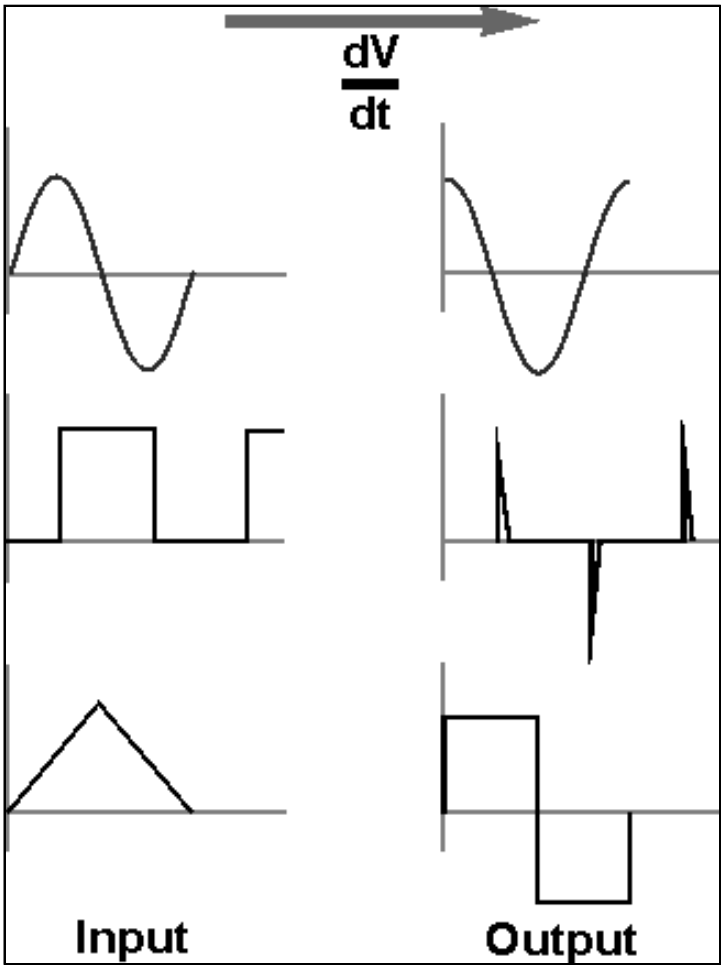


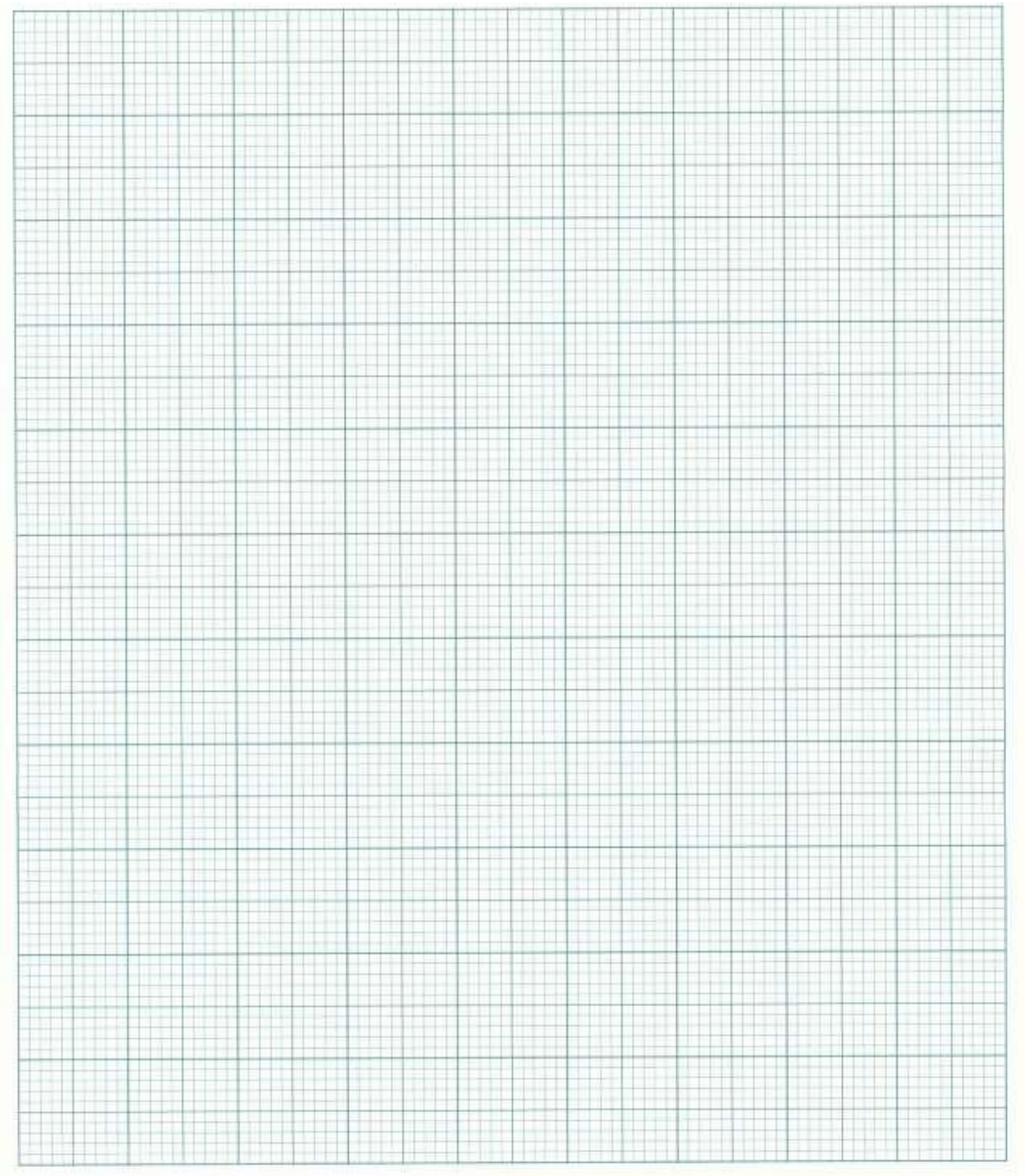
Figure: Model output waveforms for different input signals

Tabular Column:

S. No	V_{in}	V_{out}	V_{out}/V_{in}

THEORETICAL CALCULATIONS:

GRAPH SHEET:



RESULT:

EXPERIMENT-5

SUMMATION AMPLIFIER

AIM: To demonstrate Summing Amplifier Circuit using Op-Amp.

APPARATUS: 741/OP27 IC or its equivalent

10 KΩ, 1.5KΩ Resistors

Analog Discovery Kit (AD Kit)

Breadboard

THEORY:

Summing amplifier is a circuit whose output is the sum of several input signals. For example: An inverting summing amplifier with two input voltages V_1 and V_2 two input resistors R_1 and R_2 and a feedback resistor (consider all are of equal values).

$$V_o = -I_K R$$

$$= -\frac{1}{R}(V_1 + V_2) R$$

$$= -(V_1 + V_2)$$

CIRCUIT DIAGRAM:

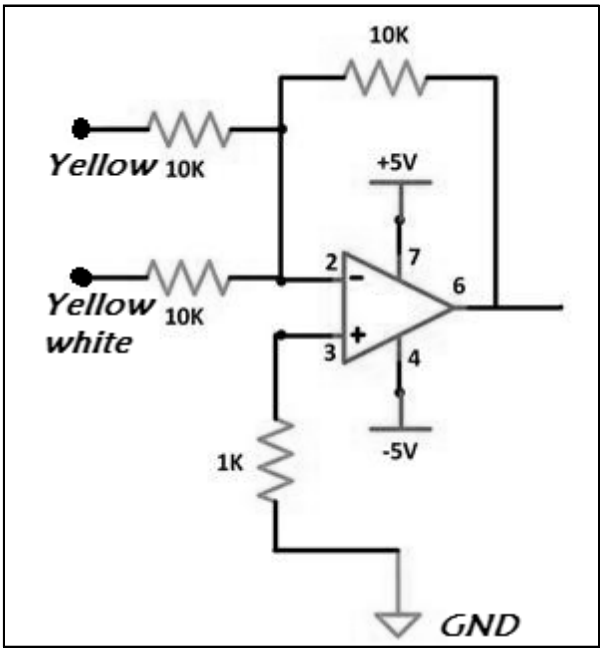


Figure: Summing Amplifier Circuit

PROCEDURE:

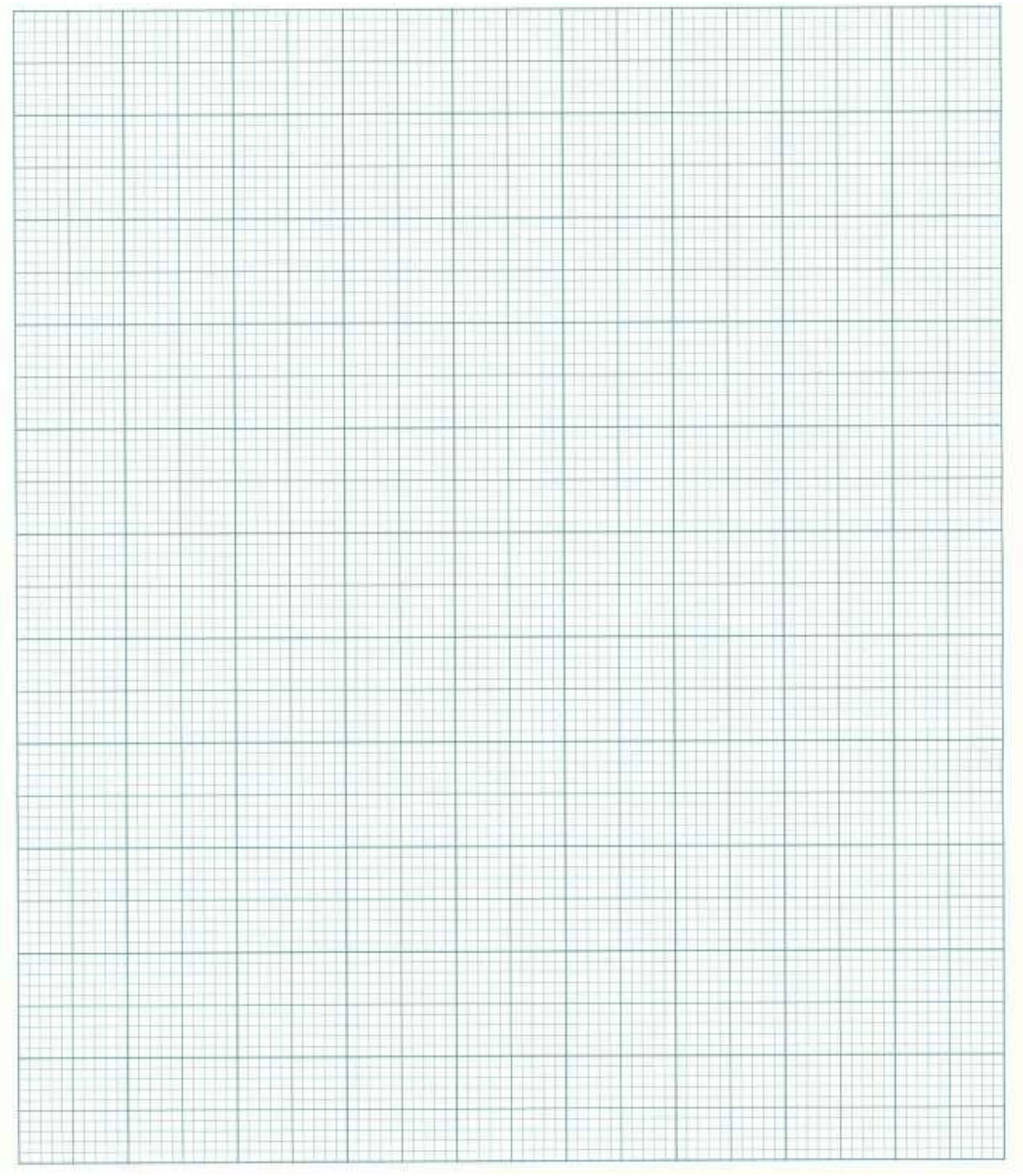
1. Connect the relevant circuit for the summing configuration as shown in the circuit diagram.
2. Measure the output voltage V_o from AD Kit.
3. Observe the waveforms at V_1, V_2, and V_o.
4. Note the phase of the output voltage V_o with respect to the input voltage.
5. Set different values of two input voltages, and find the output voltage
6. Repeat the steps 3, 4, and 5.
7. The waveforms are to be plotted.

Tabular Column:

S.No	V_{in}	V_{out}	V_{out}/V_{in}

Theoretical Calculations:

GRAPH SHEET:



RESULT:

EXPERIMENT-6
Analog Multiplier

AIM: To design a Multiplier Circuit using Op-Amp for multiplying two time varying signals.

APPARATUS: AD533or AD534 IC or its equivalent

10 KΩ, 1.5KΩ Resistors

Analog Discovery Kit (AD Kit)

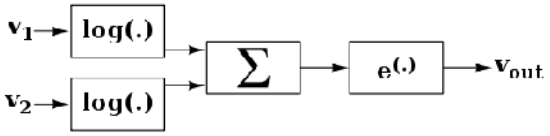
Breadboard

THEORY:

As known, using operational amplifiers and diodes it's quite easy to obtain the logarithm and the exponential of a certain input. Remembering the property of logarithms:

$$\log(a \cdot b) = \log a + \log b$$

we can multiply two signals first calculating their logarithm, then summing them and finally calculating the exponential of such a sum. From the point of view of mathematics, such an approach works as long as the two inputs are positive, because the logarithm of a negative number does not exist (in the real domain). We'll see that this limit is valid for the actual circuit as well, even if the reason will be more "physical". The block diagram of this implementation is the following:



If we simply append the circuits for logarithm, sum and exponential we get the following configuration:

For a quick overview on the behavior of the circuit, we'll assume that all the resistors *R* have the same value. It is obviously possible to use different values to get different results, but we will not consider it here. Let us use the following notation for the relationship between current and voltage on a diode:

$$i = I_s \left(e^{\frac{v}{V_T}} - 1 \right)$$

Where $V_T \simeq 0.6V$ is the threshold voltage and I_s is the current flowing through the diode if it's inverse-polarized. If we analyze the circuit without introducing any approximation we get:

$$v_a = -\left[-V_T \ln\left(\frac{v_1}{RI_s} + 1 \right) - V_T \ln\left(\frac{v_2}{RI_s} + 1 \right) \right] = V_T \ln\left[\left(\frac{v_1}{RI_s} + 1 \right) \left(\frac{v_2}{RI_s} + 1 \right) \right]$$

so the final output is:

$$v_b = -RI_s \left(e^{\frac{v_a}{V_T}} - 1 \right) = -\frac{v_1 \cdot v_2}{RI_s} - (v_1 + v_2)$$

as it is clear, in the output there is the multiplication we were looking for, but there is another term we don't want. It can't be simply considered an error because it might be as great as the

multiplication element, so it has to be removed. Anyway this is an easy task, since it is necessary only to add another stage to sum exactly$v_1 + v_2$, so we will have no error.
Where the output voltage is given by:

$$v_{out} = -\left(-\frac{v_1 \cdot v_2}{RI_s} - (v_1 + v_2) + (v_1 + v_2)\right) = \frac{v_1 \cdot v_2}{RI_s}$$

That's exactly what we wanted. The circuit works as long as the following relationship is verified:

$$v_1, v_2 > -RI_s$$

So the inputs can be zero or slightly negative but, since RI_s will be a small voltage, we are allowed to rewrite the relation simply as $v_1, v_2 \geq 0$. From the mathematical point of view this is due to the fact that we can't calculate the logarithm of a negative number, from a physical point of view the limit is due to the fact that we can obtain only very small currents (almost zero) inverse-polarizing the diodes.

In practical applications, the diodes are replaced with BJTs connected so to work like a diode.

CIRCUIT DIAGRAM:

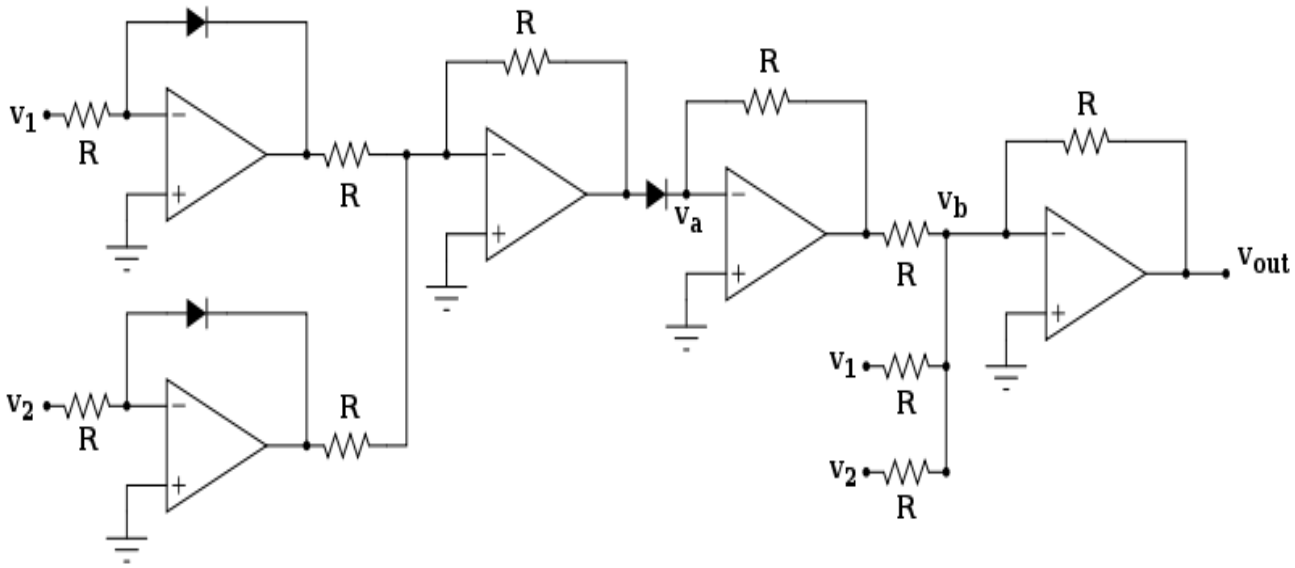


Figure: Analog Multiplier

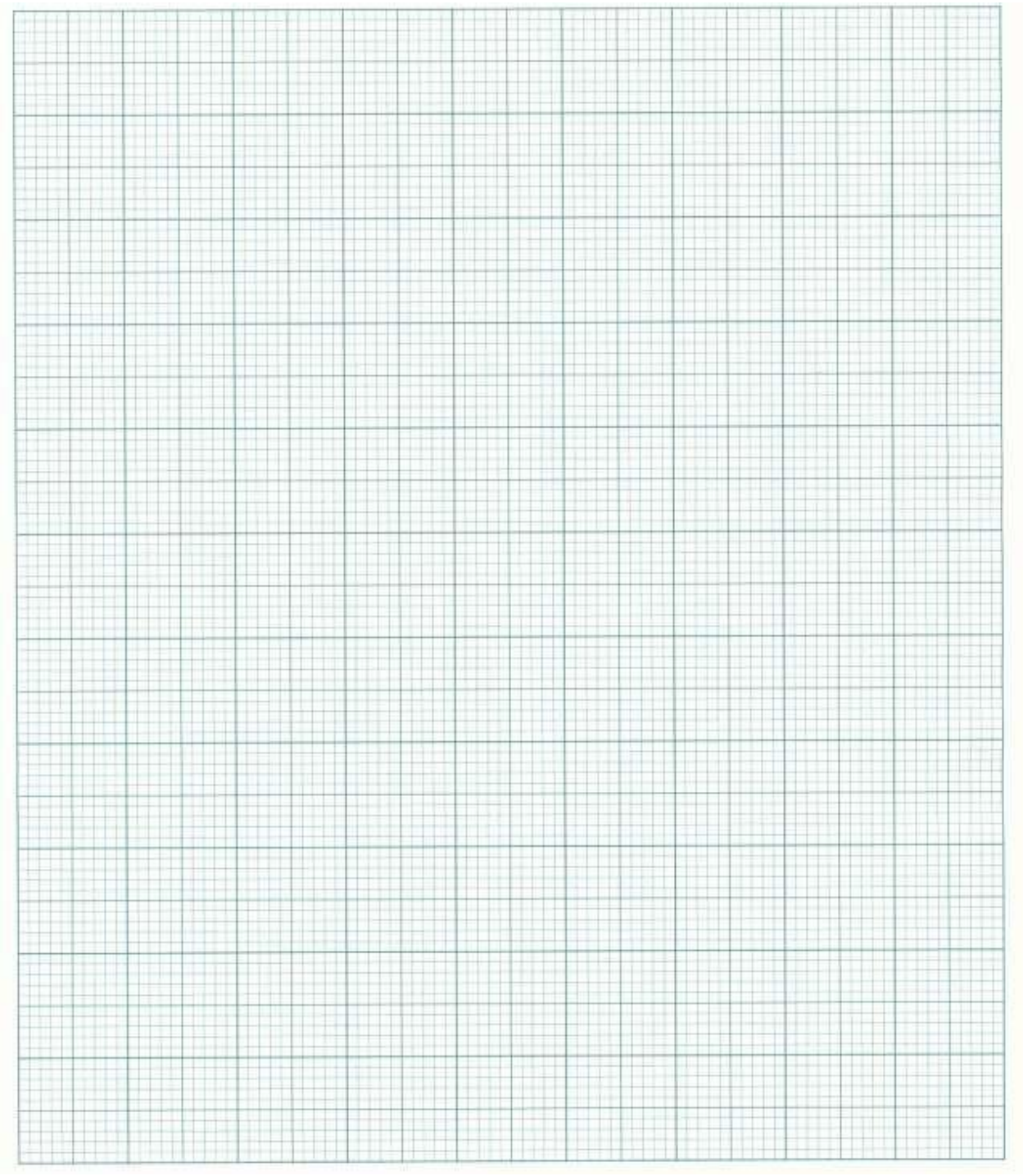
PROCEDURE:

1. Connect the relevant circuit for designing a Multiplier Circuit as shown in the circuit diagram.
2. Measure the output voltage V_o from AD Kit.
3. Observe the waveforms at V_1, V_2, and V_o.
4. Set different values of two input voltages, and find the output voltage
5. Repeat the steps 2, 3, and 4.
7. The waveforms are to be plotted.

Tabular Column:

S.No	V1	V 2	V_{out}

GRAPH SHEET:



RESULT:

EXPERIMENT-7

DIFFERENTIAL AMPLIFIER

AIM: To demonstrate Summing Amplifier Circuit using Op-Amp.

APPARATUS: 741/OP27 IC or its equivalent (1)

Resistors 2.2KΩ, 10KΩ

Analog Discovery Kit (AD Kit)

Breadboard

CIRCUIT DIAGRAM:

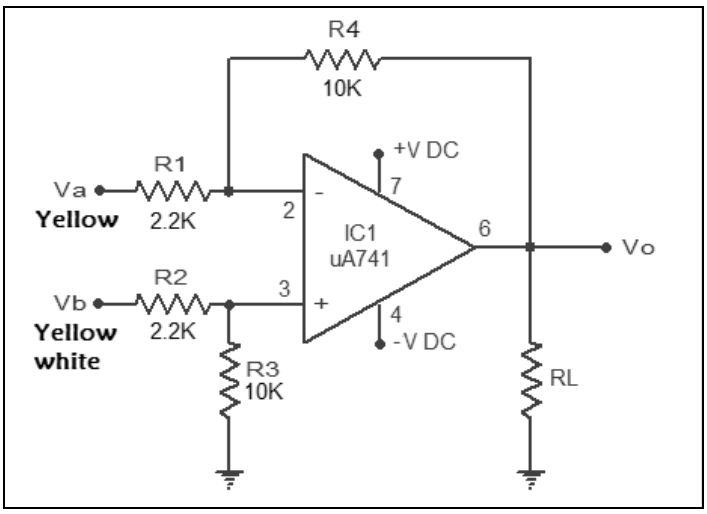


Figure: Differential Amplifier

THEORY:

The *differential amplifiers* amplify the difference between two voltages making this type of operational amplifier circuit a Subtractor unlike a summing amplifier which adds or sums together the input voltages. This type of operational amplifier circuit is commonly known as a Differential Amplifier configuration.

By connecting each input in turn to 0v ground we can use superposition to solve for the output voltage V_{out}. Then the transfer function for a Differential Amplifier circuit is given as:

$$V_{out} = -V_1\left(\frac{R_3}{R_1}\right) + V_2\left(\frac{R_4}{R_2+R_4}\right)\left(\frac{R_1+R_3}{R_1}\right)$$

When resistors, R1 = R2 and R3 = R4 the above transfer function for the differential amplifier can be simplified to the following expression:

$$V_{OUT} = \frac{R_3}{R_1}\left(V_2 - V_1\right)$$

If all the resistors are all of the same ohmic value, that is: R1 = R2 = R3 = R4 then the circuit will become a **Unity Gain Differential Amplifier** and the voltage gain of the amplifier will be exactly one or unity. Then the output expression would simply be Vout = V2 - V1. Also note that if input V1 is higher than input V2 the output voltage sum will be negative, and if V2 is higher than V1, the output voltage sum will be positive.

The Differential Amplifier circuit is a very useful op-amp circuit and by adding more resistors in parallel with the input resistors R1 and R3, the resultant circuit can be made to either "Add" or "Subtract" the voltages applied to their respective inputs. One of the most common ways of doing this is to connect a "Resistive Bridge" commonly called a *Wheatstone Bridge*

PROCEDURE:

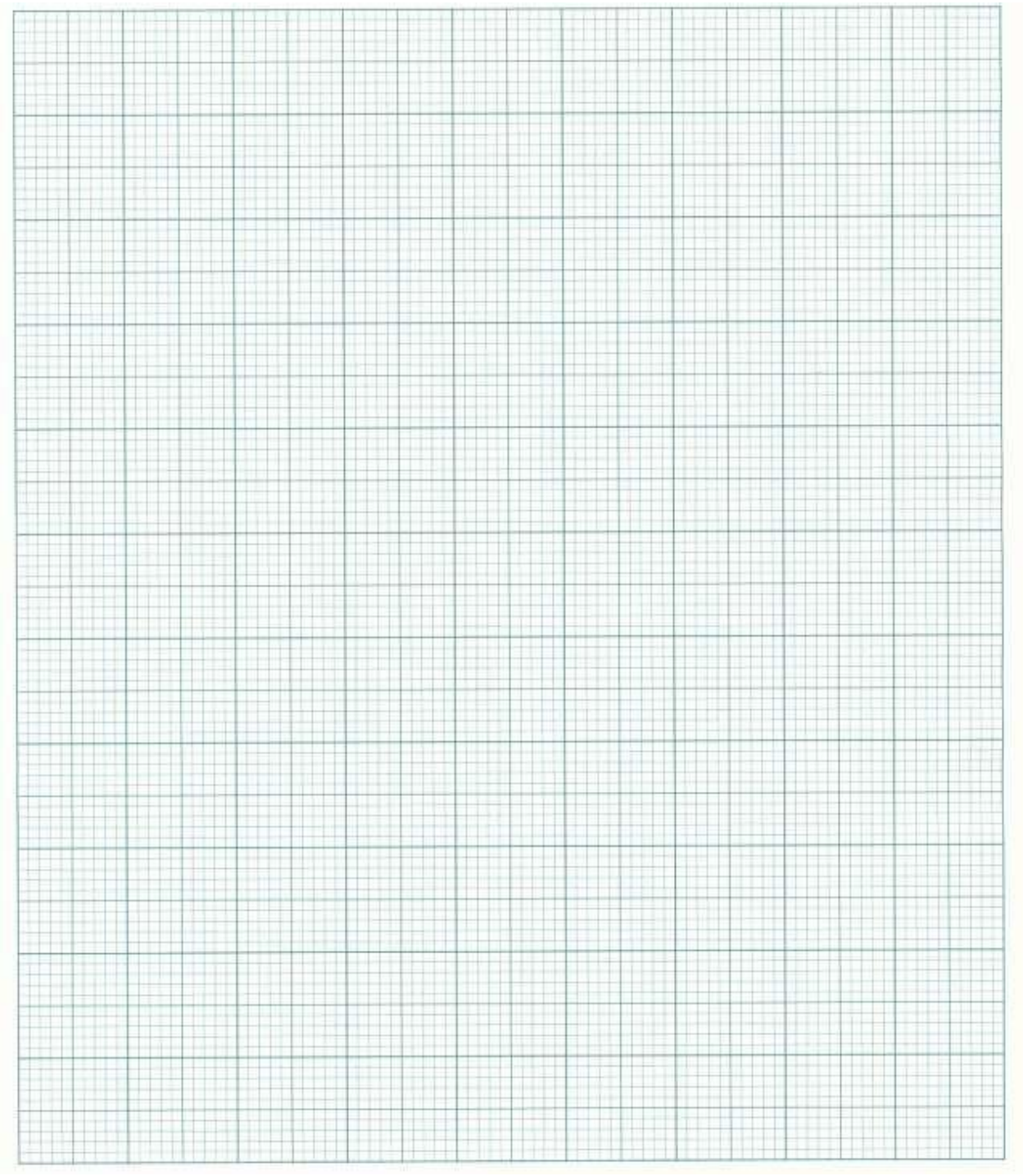
1. Connect the relevant circuit for the difference configuration as shown in the circuit diagram.
2. Measure the output voltage V_o from AD Kit.
3. Observe the waveforms at V_1, V_2, and V_o.
4. Note the phase of the output voltage V_o with respect to the input voltage.
5. Set different values of two input voltages, and find the output voltage
6. Repeat the steps 3, 4, and 5.
7. The waveforms are to be plotted.

Tabular Column:

S.No	**V_{in}**	**V_{out}**	**V_{out}/V_{in}**

<u>Theoritical Calculations</u>:

GRAPH SHEET:



RESULT:

EXPERIMENT-8

SQUAREWAVE GENERATOR

AIM: To construct and demonstrate square wave generator using op-amp.

APPARATUS:
LM 741/OP27 or its equivalent

Capacitor – 0.1μF

Resistors – 10KΩ (2), 1KΩ (2)

AD Kit

Bread Board.

THEORY:

The non-sinusoidal waveform generators are also called relaxation oscillators. The op-amp relaxation oscillator shown in figure is a square wave generator. In general, square waves are relatively easy to produce.

The comparator uses positive feedback that increases the gain of the amplifier. In a comparator circuit this offer two advantages. First, the high gain causes the op-amp's output to switch very quickly from one state to another and vice-versa. Second, the use of positive feedback gives the circuit hysteresis. In the op-amp square-wave generator circuit given in figure, the output voltage v_{out} is shunted to ground by two Zener diodes Z_1 and Z_2 connected back-to-back and is limited to either $V_{Z\,2}$ or $-V_{Z\,1}$. A fraction of the output is fedback to the non-inverting (+) input terminal. Combination of IL and C acting as a low-pass R-C circuit is used to integrate the output voltage v_{out} and the capacitor voltage v_c is applied to the inverting input terminal in place of external signal. The differential input voltage is given as $\mathbf{v_{in} = v_c - \beta\, v_{out}}$

When v_{in} is positive, $v_{out} = -V_{z1}$ and when v_{in} is negative $v_{out} = +V_z 2$. Consider an instant of time when $v_{in} < 0$. At this instant $v_{out} = +V_{z\,2}$, and the voltage at the non-inverting (+) input terminal is $\beta V_{z\,2}$, the capacitor C charges exponentially towards $V_{z\,2}$, with a time constant $R_f C$. The output voltage remains constant at $V_{z\,2}$ until v_c equal $\beta V_{z\,2}$.

When it happens, comparator output reverses to $-V_{z\,1}$. Now v_c changes exponentially towards $-V_{z1}$ with the same time constant and again the output makes a transition from $-V_{z1}$ to $+V_{z\,2.}$ when v_c equals $-\beta V_{z\,1}$

Let $V_{z1} = V_{z\,2}$

The time period, T, of the output square wave is determined using the charging and discharging phenomena of the capacitor C. The voltage across the capacitor, v_c when it is charging from $-\beta V_z$ to $+V_z$ is given by

$\mathbf{V_c = [1-(1+\beta)]e^{-T/2\tau}}$

Where $\tau = R_fC$

The waveforms of the capacitor voltage v_c and output voltage v_{out} (or v_z) are shown in figure.

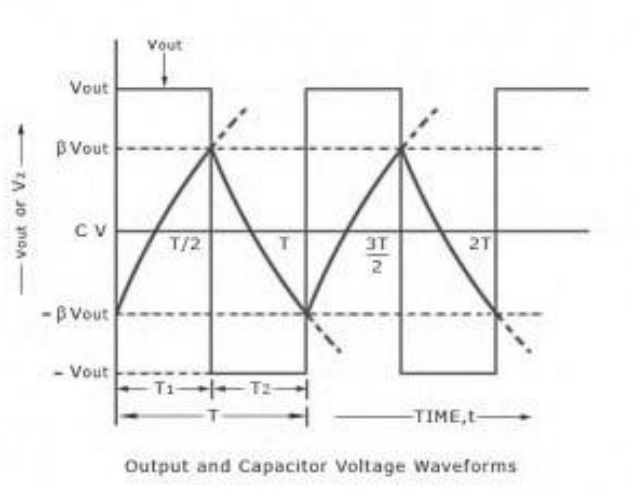
When t = t/2

$\mathbf{V_c = +\beta\ V_{z\ or} + \beta\ V_{out}}$

Therefore $\beta\ V_z = V_z\,[1-(1+\beta)e^{-T/2\tau}]$

$\mathbf{Or\ e^{-T/2\tau} = 1-\beta/1+\beta}$

$\mathbf{Or\ T = 2\tau\ log_e\ 1+\beta/1-\beta = 2R_f\,C\ log_e\,[1+(2R_3/R_2)]}$



Output and Capacitor Voltage Waveforms

The frequency, f = 1/T , of the square-wave is independent of output voltage V_{out}. ***This circuit is also known as free-running or astable multivibrator because it has two quasi-stable states***. The output remains in one state for time T_1 and then makes an abrupt transition to the second state and remains in that state for time T_2. The cycle repeats itself after time $\mathbf{T = (T_1 + T_2)}$ where T is the time period of the square-wave.

The op-amp square-wave generator is useful in the frequency range of about 10 Hz -10 kHz. At higher frequencies, the op-amp's slew rate limits the slope of the output square wave. The symmetry of the output waveform depends on the matching of two Zener diodes Z_1 and Z_2. The unsymmetrical square-wave (T_1 not equal to t_2) can be had by using different constants for charging the capacitor C to $+V_{out}$ and $-V_{out}$

CIRCUIT DIAGRAM:

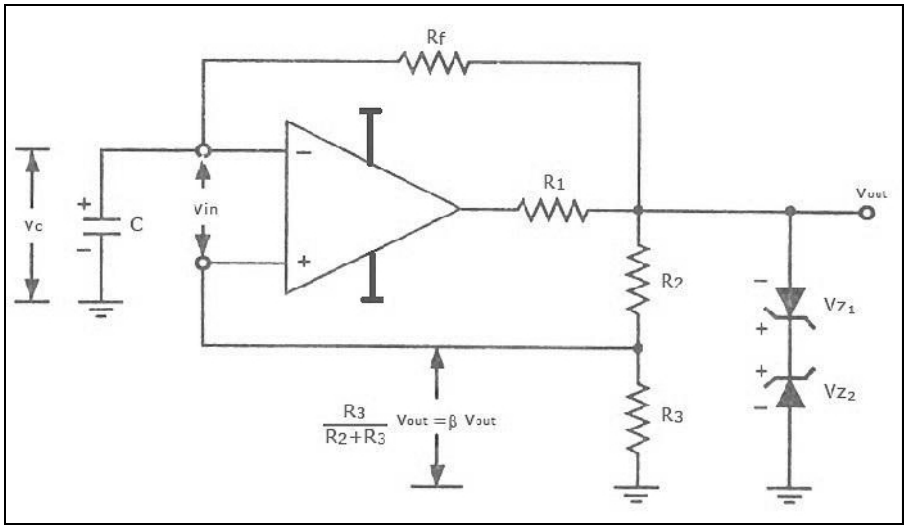


Figure: Circuit diagram for square wave generator

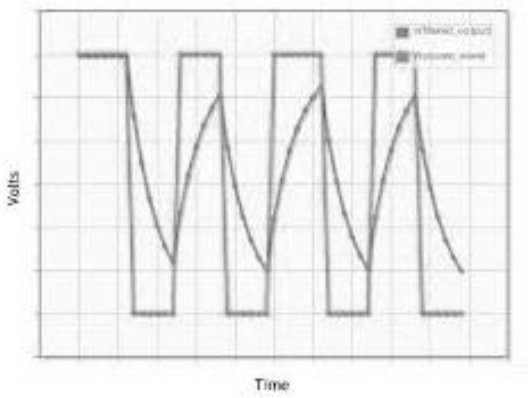
PROCEDURE:

1. Expression for the frequency of oscillation,

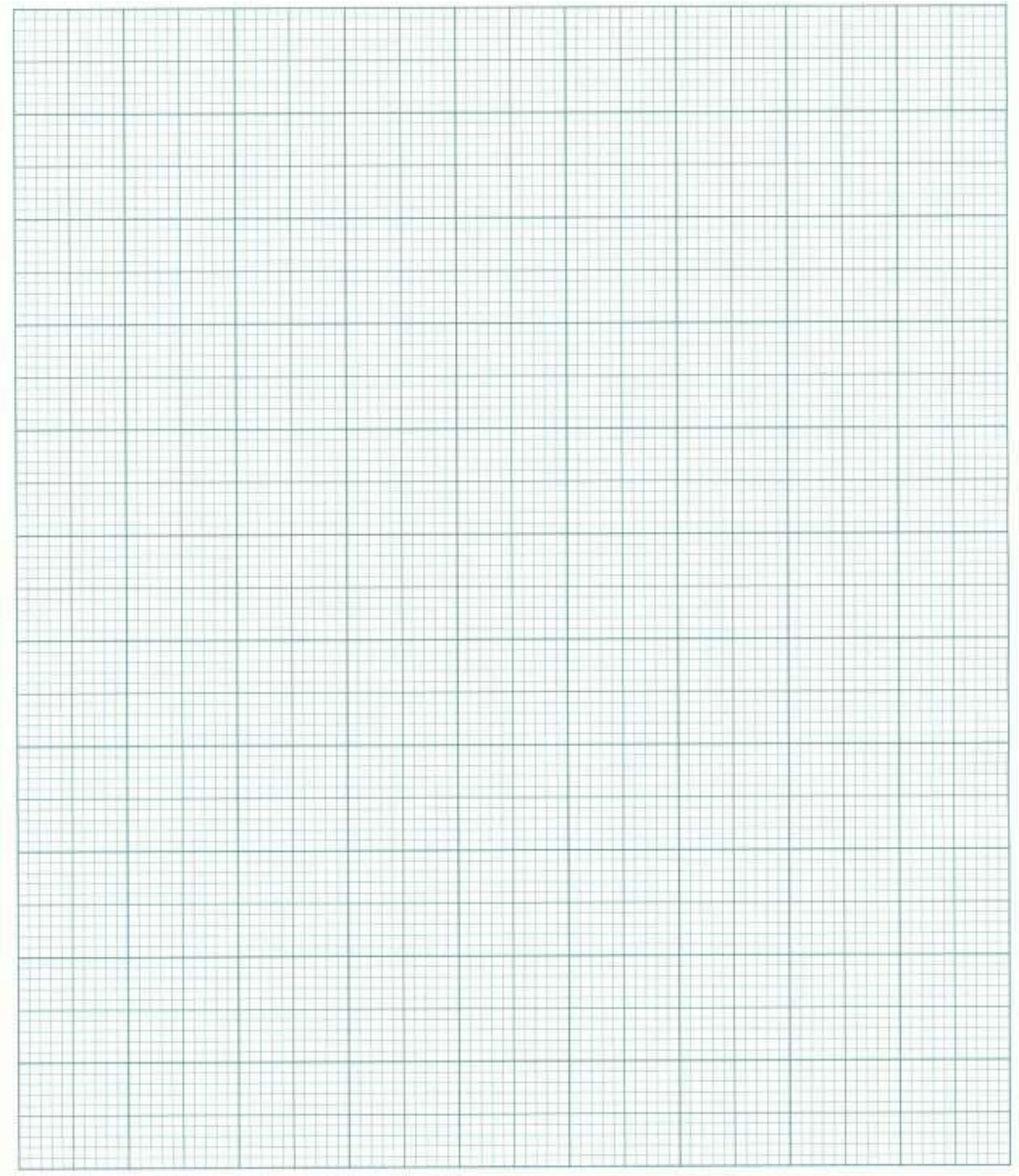
$$f = 1/ (2RC\log_e (1+ \beta/1-\beta)), \text{ where } \beta = (R_3/R_3+R_2).$$

2. Choose any frequency between 1 kHz and 5 kHz and select the values of R_1, R_2, R, and C.
3. Connect the circuit as per the circuit diagram and give the supply voltage.
4. Observe the frequency of operation of the circuit and compare with the theoretical values.
5. Change the R and C values to change the frequency and oscillation and verify with the theoretical values.
6. Trace the output waveform for inverting and non-inverting inputs.

MODEL GRAPHS:



GRAPH SHEET:



RESULT:

Exercise:

1. Write a short notes on types of oscillators and their applications

EXPERIMENT-9

TRIANGULAR WAVE GENERATOR

AIM: To construct and demonstrate Triangular wave generator using LM741/OP27.

APPARATUS:
LM741/OP27 or its equivalent

Resistors – 10kΩ (2), 22kΩ, 47kΩ

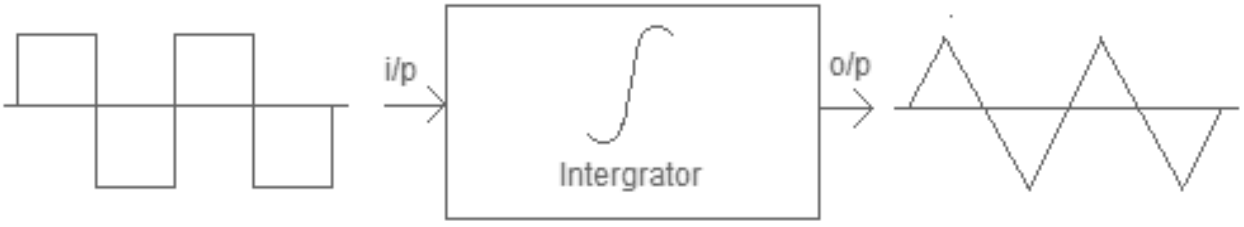
Capacitor – 0.1µF

Analog discovery Kit (AD Kit)

Bread Board

THEORY:

This experiment is about a triangular wave generator using opamp IC. Triangular wave is a periodic, non-sinusoidal waveform with a triangular shape. People often get confused between triangle and sawtooth waves. The most important feature of a triangular wave is that it has equal rise and fall times while a sawtooth wave has un-equal rise and fall times. The applications of triangular wave include sampling circuits, thyristor firing circuits, frequency generator circuits, tone generator circuits etc. There are many methods for generating triangular waves but here we focus on method using opamps. This circuit is based on the fact that a square wave on integration gives a triangular wave.



Generating triangular wave from a square wave

The circuit uses an opamp based square wave generator for producing the square wave and an opamp based integrator for integrating the square wave. The circuit diagram is shown in the figure. The square wave generator section and the integrator section of the circuit is explained in detail.

Square wave generator:

The square wave generator is based on a uA741 opamp (IC1). Resistor R_1 and capacitor C_1

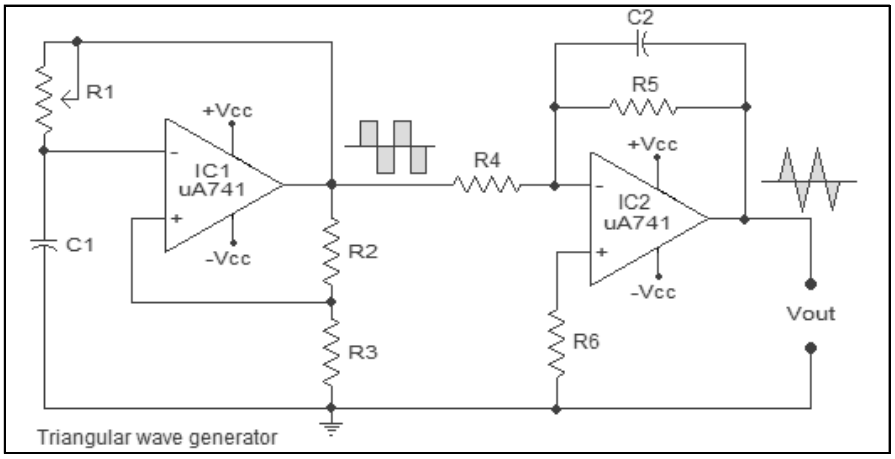


Figure: Circuit diagram of Triangular wave generator

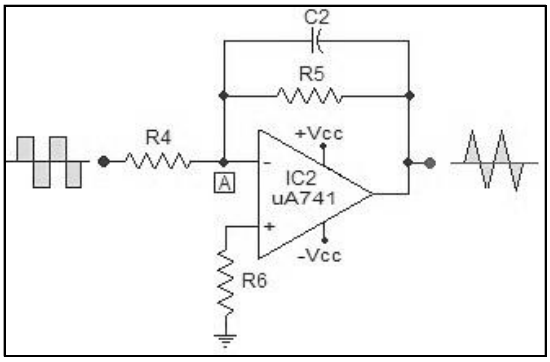
determines the frequency of the square wave. Resistor R_2 and R_3 forms a voltage divider setup which feedbacks a fixed fraction of the output to the non-inverting input of the IC.

Initially, when power is not applied the voltage across the capacitor C_1 is 0V. When the power supply is switched ON, the C1 starts charging through the resistor R_1 and the output of the opamp will be high (+Vcc). A fraction of this high voltage is fed back to the non- inverting pin by the resistor network R_2, R_3. When the voltage across the charging capacitor is increased to a point the the voltage at the inverting pin is higher than the non-inverting pin, the output of the opamp swings to negative saturation (-Vcc). The capacitor quickly discharges through R_1 and starts charging in the negative direction again through R_1. Now a fraction of the negative high output (-Vcc) is fed back to the non-inverting pin by the feedback network R_2, R_3. When the voltage across the capacitor has become so negative that the voltage at the inverting pin is less than the voltage at the non-inverting pin, the output of the opamp swings back to the positive saturation. Now the capacitor discharges trough R_1 and starts charging in positive direction. This cycle is repeated over time and the result is a square wave swinging between +Vcc and -Vcc at the output of the opamp. If the values of R_2 and R_3 are made equal, then the frequency of the square wave can be expressed using the following equation:

$$F=1 / (2.1976 R_1C_1)$$

Integrator:

Next part of the triangular wave generator is the opamp integrator. Instead of using a simple passive RC integrator, an active integrator based on opamp is used here. The opamp IC used in this stage is also uA741 (IC2). Resistor R_5 in conjunction with R4 sets the gain of the integrator and resistor R_5 in conjunction with C_2 sets the bandwidth. The square wave signal is applied to the inverting input of the opamp through the input resistor R_4. The opamp integrator part of the circuit is shown in the figure below.

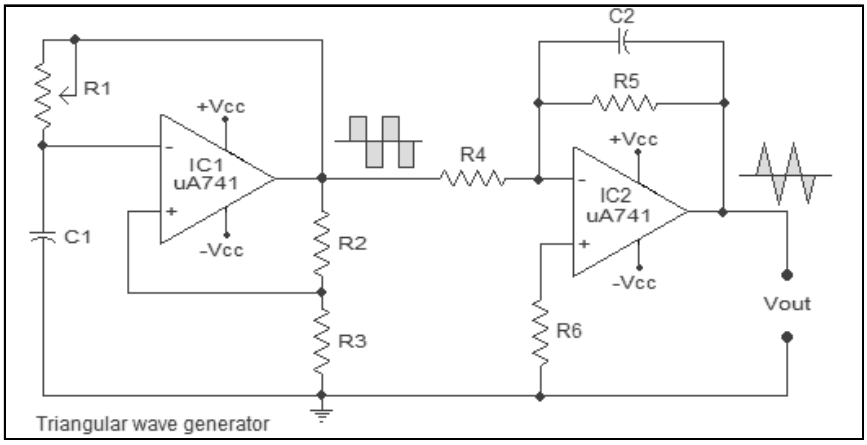


Let's assume the positive side of the square wave is first applied to the integrator. By virtue capacitor C_2 offers very low resistance to this sudden shoot in the input and C_2 behaves something like a short circuit. The feedback resistor R_5 connected in parallel to C_2 can be put aside because R_5 has almost zero resistance at the moment. A serious amount of current flows through the input resistor R_4 and the capacitor C_2 bypasses all these current. As a result the inverting input terminal (tagged A) of the opamp behaves like a virtual ground because all the current flowing into it is drained by the capacitor C_2. The gain of the entire circuit (Xc_2/R_4) will be very low and the entire voltage gain of the circuit will be close the zero.

After this initial "kick" the capacitor starts charging and it creates an opposition to the input current flowing through the input resistor R_4. The negative feedback compels the opamp to produce a voltage at its out so that it maintains the virual ground at the inverting input. Since the capacitor is charging its impedance Xc keeps increasing and the gain Xc_2/R_4 also keeps increasing. This results in a ramp at the output of the opamp that increases in a rate proportional to the RC time constant ($T=R_4C_2$) and this ramp increases in amplitude until the capacitor is fully charged.

When the input signal (square wave) falls to the negative peak at integrator, the capacitor quickly discharges through the input resistor R_4, and starts charging in the opposite polarity. Now the conditions are reversed and the output of the opamp will be a ramp that is going to the negative side at a rate proportional to the R_4R_2 time constant. This cycle is repeated and the result will be a triangular waveform at the output of the opamp integrator.

CIRCUIT DIAGRAM:



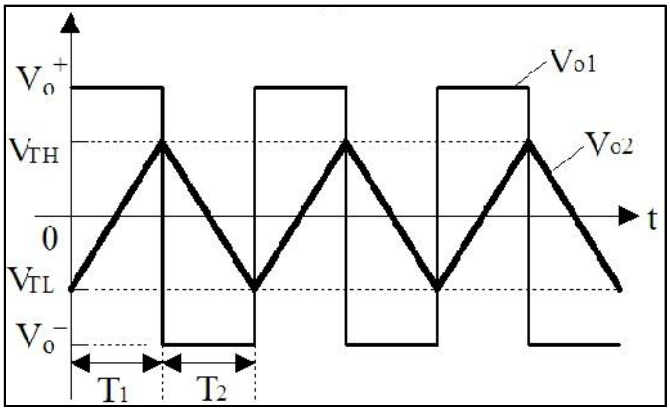
PROCEDURE:

1. Connect the components on the bread board as shown in the Circuit diagram
2. Connect the AD kit and find the output voltage and its frequency of the circuit connected on the Bread board
3. Calculate the frequency by changing the value of R_1.
4. Tabulate the values taken and write the frequency obtained
5. Plot the graph of output voltage considering both square and triangular waves.

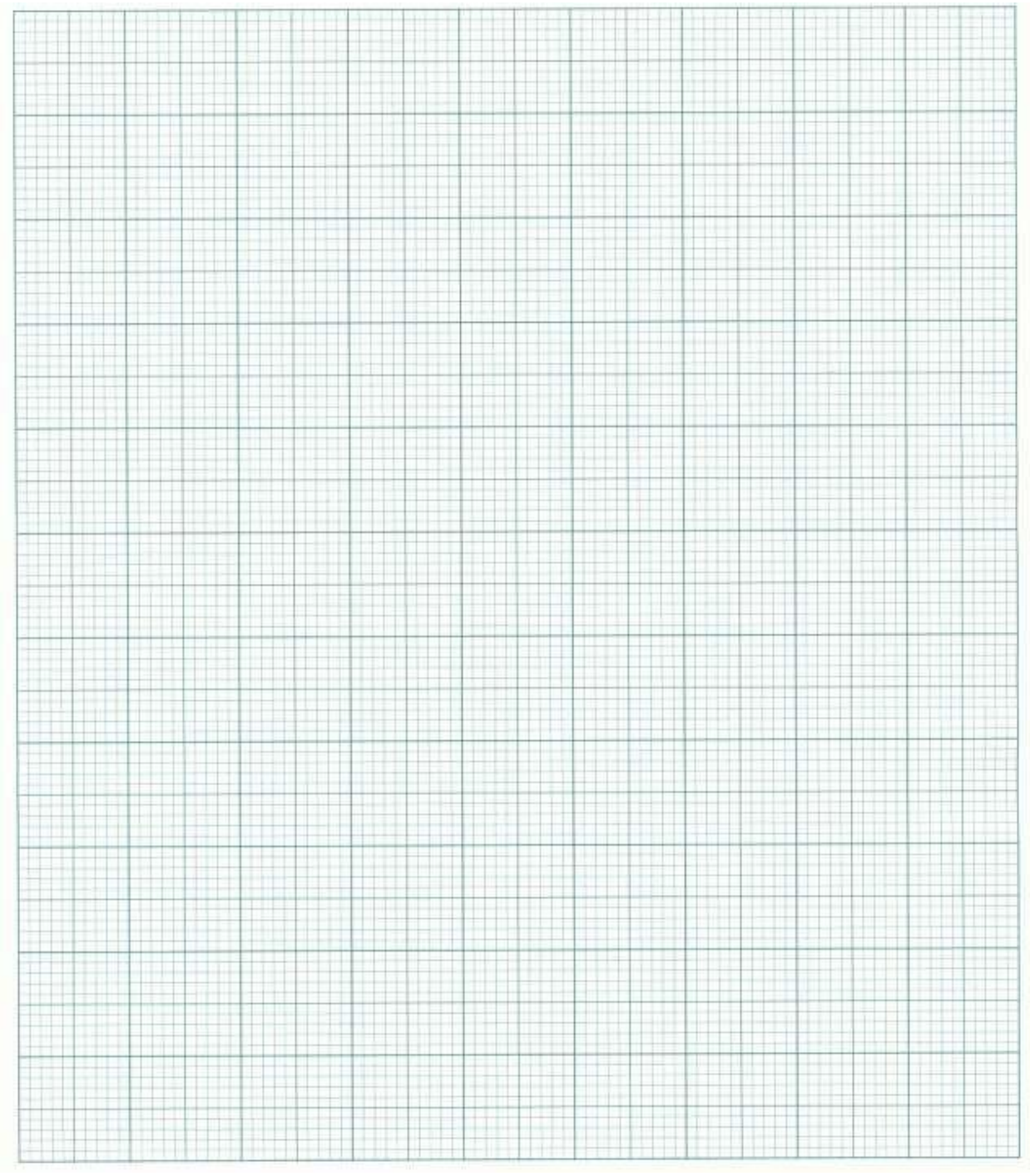
Tabular Column:

S.No	$R_2(k\Omega)$	Frequency

MODEL GRAPH:



GRAPH SHEET:



RESULT:

EXPERIMENT-10
SINE WAVE GENERATOR

AIM: To construct and demonstrate Sine wave generator using LM741/OP27.

APPARATUS: LM741/OP27 or its equivalent
Resistors – 1.5KΩ (2), 1KΩ, 4.7KΩ potentiometer

Capacitor – 10nF (2)

Analog discovery Kit (AD Kit)

Bread Board

CIRCUIT DIAGRAM

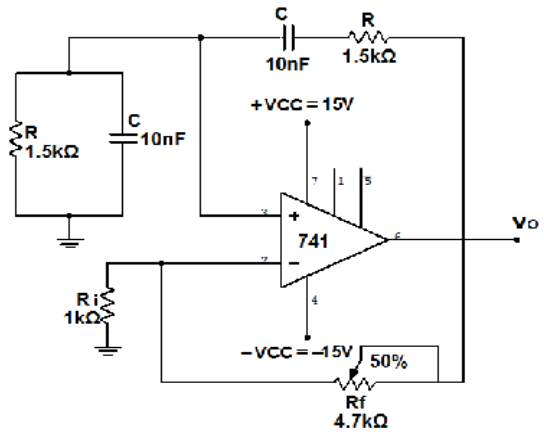


Figure: Sine wave generator Circuit

THEORY:

The **AM modulation** is a kind of modulation technique which is in use since the very early days of wireless data transmission. In a radio transmission system there is a relation between the ranges of frequencies which can be transmitted wirelessly with the length of the transmitting antenna. The relation is inversely proportional to one another, means as the frequency of the signal to be transmitted increases the length of the antenna can be reduced and as the frequency of the signal to be transmitted decreases the length of the transmitting antenna should be increased accordingly.

Using an antenna of few meters the frequencies in the range of Mhz can be easily transmitted to a distance. The basic purpose of the wireless transmitting system in early days was to transmit the audio signals, but to transmit audio signals which fall in the range of few Khz an antenna of more than a kilometer height would have been required. Since it was practically impossible to construct such a long antenna, the high frequency signals are transmitted after they are modulated with the low frequency audio signals.

The amplitude modulation is the simplest modulation technique among the wide verity of modulation techniques in use. The amplitude modulation of a high frequency signal is easy to achieve and the demodulation is also simple compared to other techniques. The high frequency signal which is modulated to carry the low frequency audio signals are called 'carrier frequency' and the audio signals used for modulation is called 'modulating signal' or 'message signal' or 'base band signal'.

*Variable frequency sine wave generator:*The sine wave generation circuit used in this project is the Wien bridge oscillator circuit. This is the only circuit which can generate the pure sine wave without any distortion. The amplifier component used in the Wien bridge circuit is an op-amp with dual-power supply. Both the circuits are built around the versatile op-amp IC, 741. The circuit of the sine wave generator is shown

The frequency of the above circuit can be varied by simply varying the potentiometer R2 and the amplitude of the wave form can be adjusted by varying the potentiometer R. The frequency of the sine wave generated by the above circuit depends on the components R1, R2, C1 and C2 and the equation for the frequency is given

$$F = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

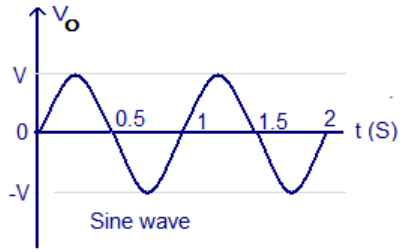
PROCEDURE:

1. Connect the components on the bread board as shown in the Circuit diagram
2. Connect the AD kit and find the output voltage and its frequency of the circuit connected on the Bread board for different values of Resistance
3. Calculate the frequency by changing the value of R_2.
4. Tabulate the values taken and write the frequency obtained
5. Plot the graph of output voltage of sine wave.

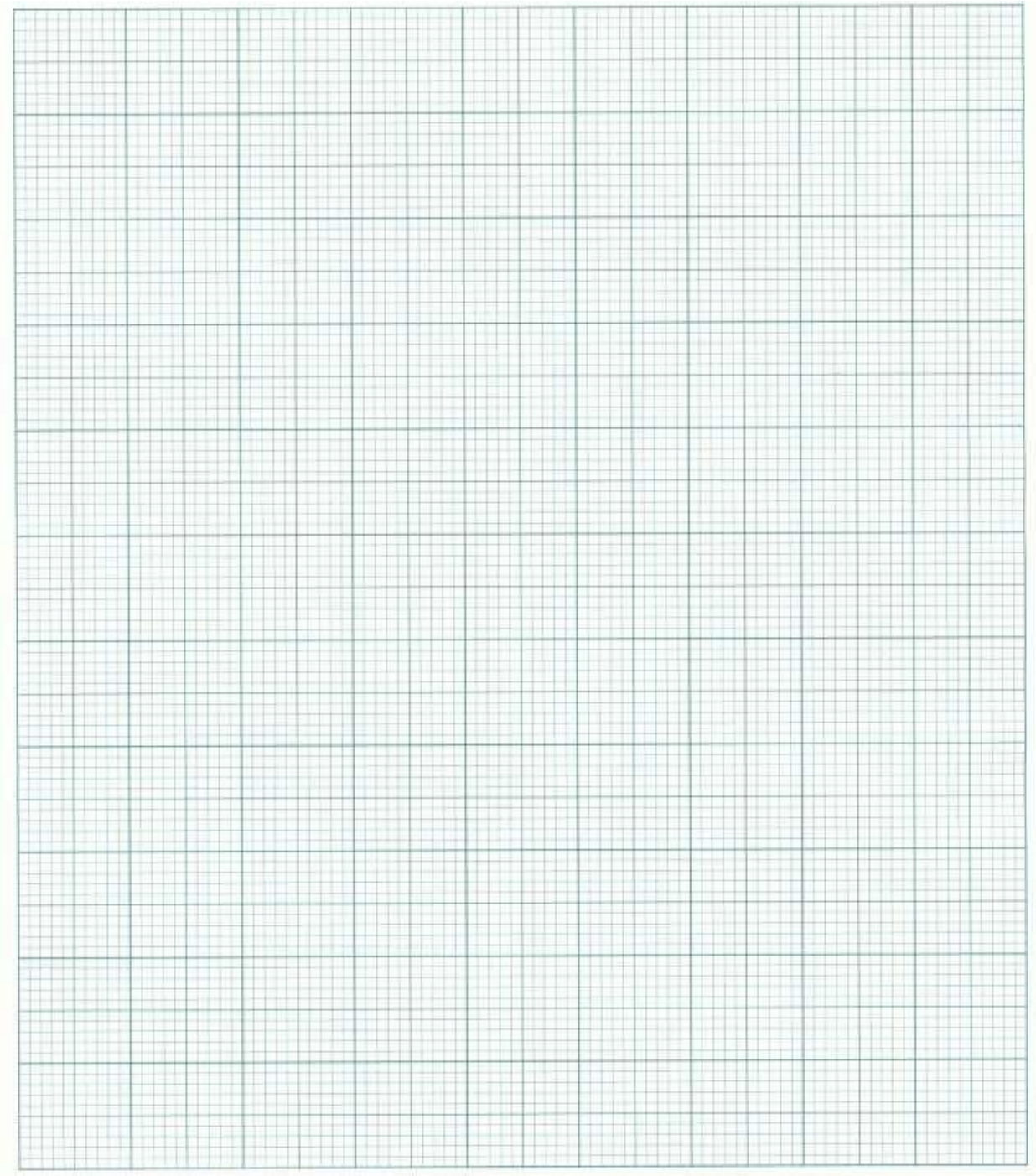
Tabular Column:

S.No	R_2(kΩ)	Frequency

MODEL GRAPH:



GRAPH SHEET:



RESULT:

Exercise:

1. Write the applications of Sine wave generator

EXPERIMENT-11

DIGITAL TO ANALOG CONVERTER

(R-2R LADDER METHOD)

AIM: To construct a 4-bit R-2R ladder type of digital to analog converter for R = 1K.

APPARATUS:

Operational Amplifier – LM741/OP 27 or its equivalent

Resistors – 1kΩ, 2.2kΩ (3), 3.3kΩ (3)

Analog Discovery Kit

Bread Board

CIRCUIT DIAGRAM:

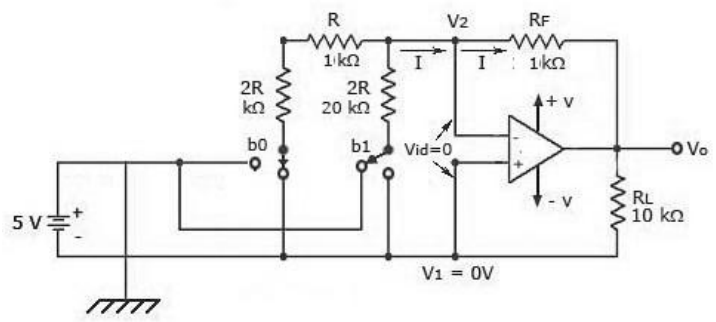


Figure: R-2R Ladder Diagram for D to A converter

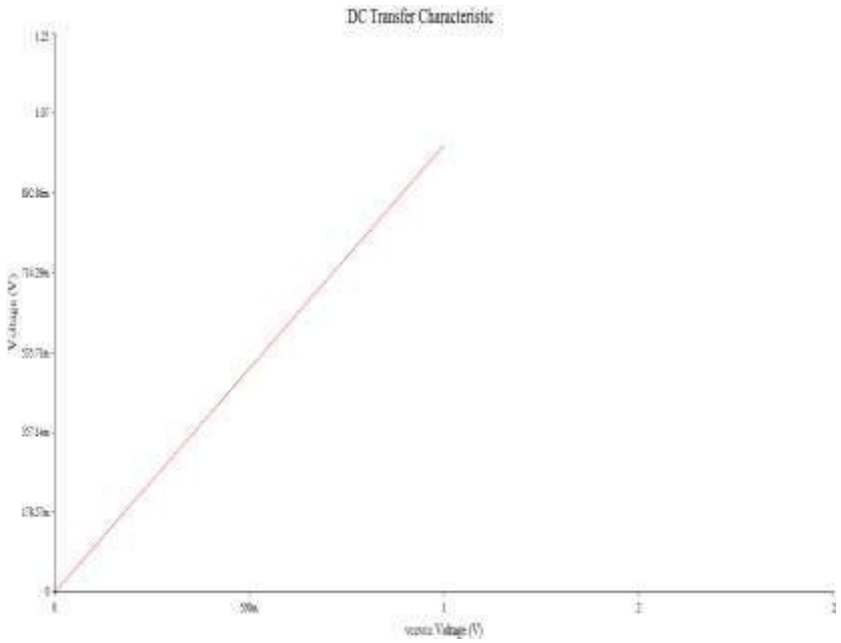
THEORY:

R-2R ladder DAC, avoids the use of wide range of resistors. This makes the circuit suitable for monolithic fabrication. Typical range of values of R will be in 2-10KΩ.

PROCEDURE:

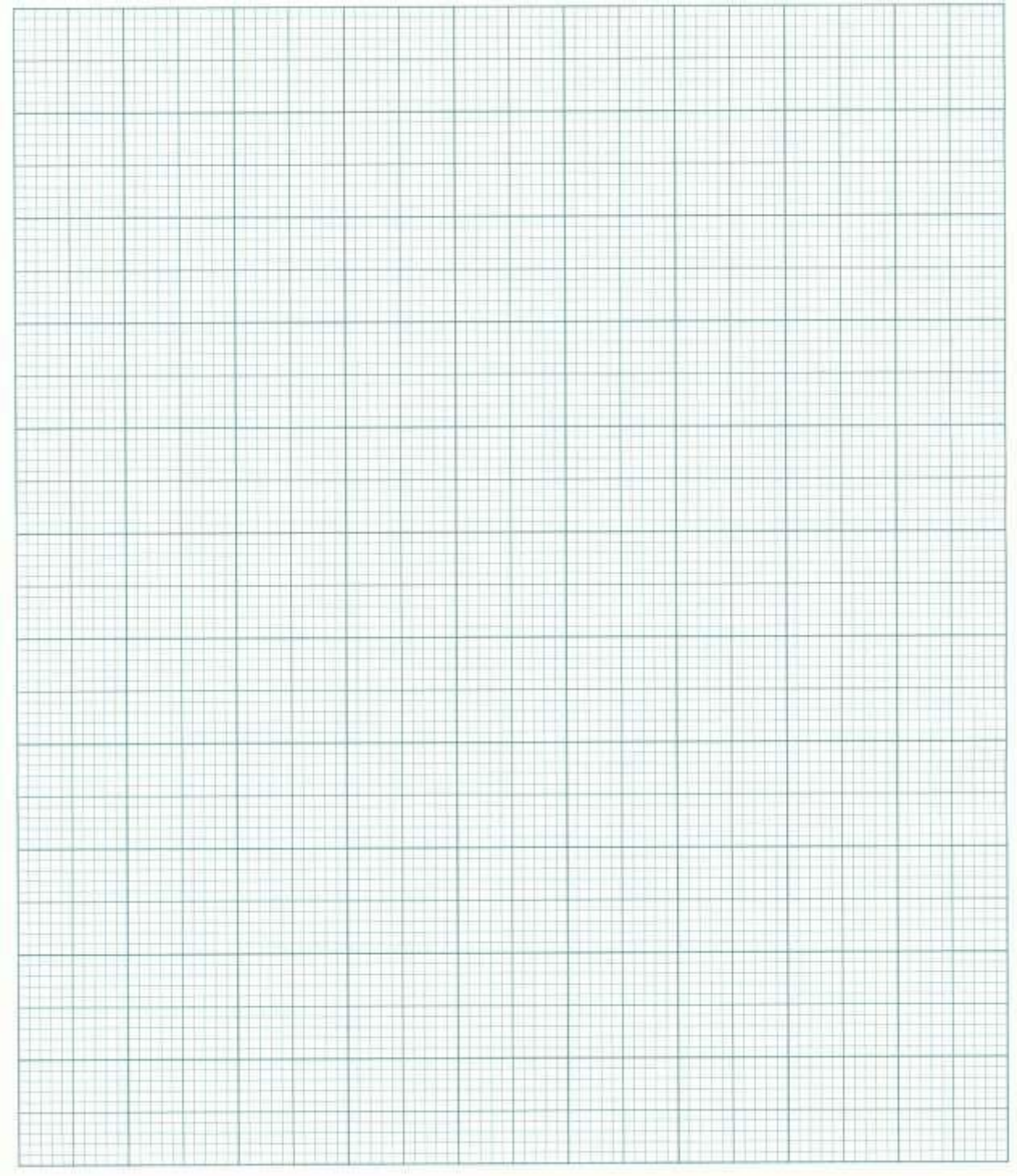
1. Set up the circuit as shown in the circuit diagram.
2. Apply the digital input of two bit and measure the analog output voltage for each of the possible combinations.
3. Plot the digital input versus the analog output voltage using AD kit.
4. Calculate the maximum linearity error and accuracy. Specify the percentage resolution.

MODEL GRAPH:



Theoretical Calculations:

GRAPHSHEET:



RESULT:

Exercise:

1. Write types of Digital to Analog converters and their applications.

EXPERIMENT-12

ASTABLE MULTIVIBRATOR USING A 555 TIMER

AIM: To design an Astable Multivibrator using a 555 timer

APPARATUS:
Operational Amplifier – 555/565 Timer
Capacitors – 10µF, 0.01µF
Resistors – 4.7kΩ, 100kΩ (variable), 1kΩ, 330Ω
LED (Optional)
Analog Discovery Kit (AD Kit)
Bread Board.

CIRCUIT DIAGRAM:

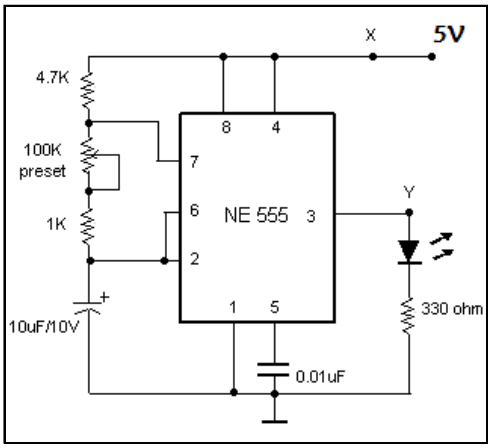


Figure: Astable Multivibrator using 555 timer

THEORY:

An astable multivibrator, also known as "free running multivibrator" is nothing but an oscillator that generates square waves. These waves are required to control the timing circuits. These multivibrator circuits can be designed using an op-amp.

An astable multivibrator designed using a 555-Timer op-amp is shown. To explain the principle operation, the internal circuit diagram of 555 Timer is also shown beside.

$$f = \frac{1.44}{(R1 + 2R2)C}$$

PROCEDURE:

1. Calculate the values of R, R, and C for different duty cycles using the formulae given.
2. Connect the circuit as per the diagram.
3. Calculate the frequency of the astable multivibrator by noting the waveform and compare it with the theoretical values.
4. Change the value of R and C to change the frequency of oscillation and verify the theoretical values.
5. Note the output voltages at pin no. 3 and capacitor voltage at pin no.6 and plot it on a graph sheet.

MODEL GRAPH:

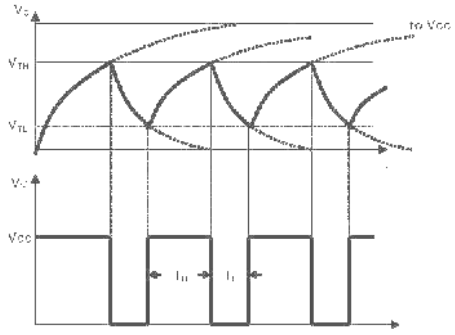


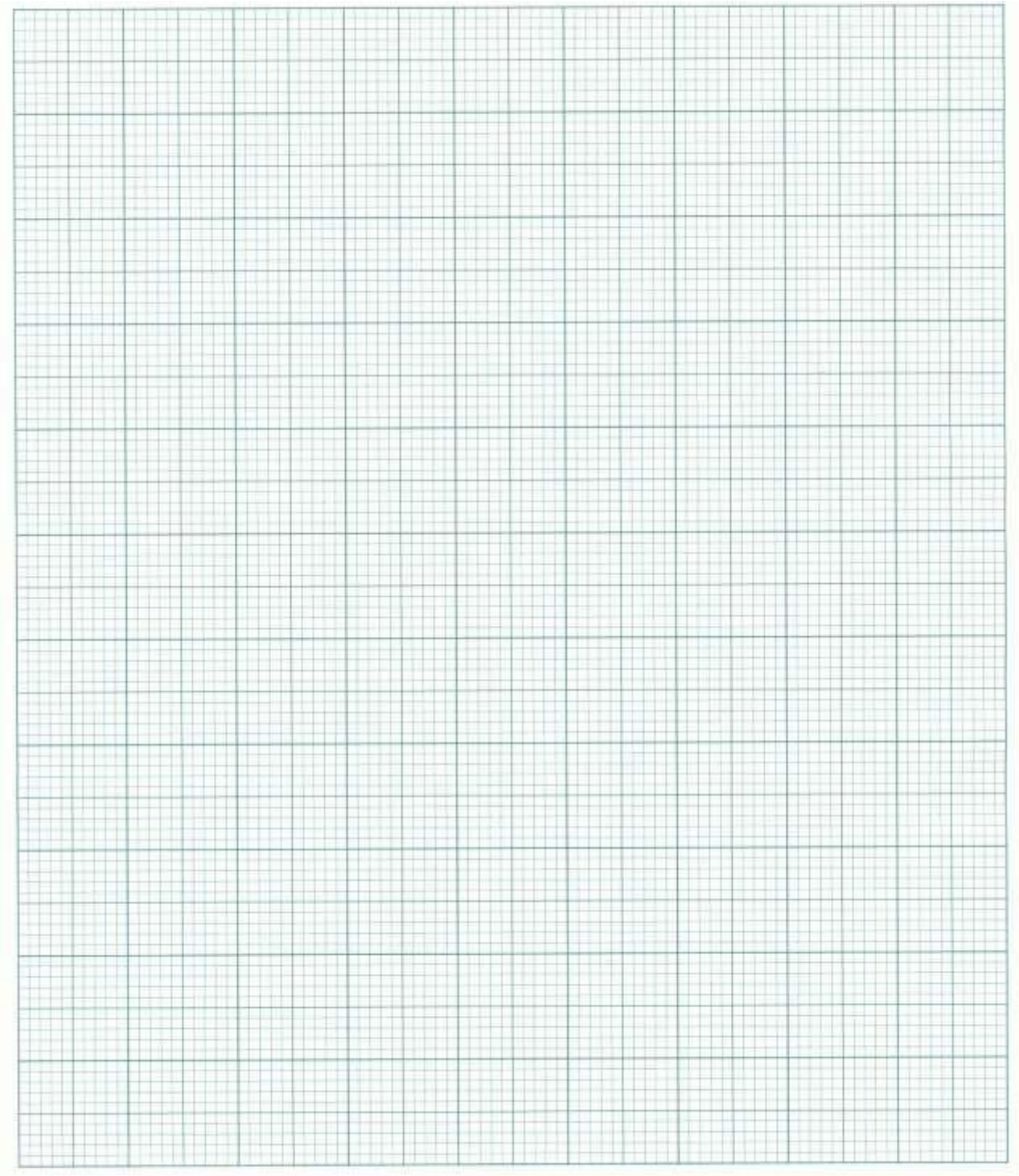
Figure: Model graphs of Astable Multivibrator

OBSERVATIONS:

S N0.	%Duty Cycle	Theoretical Frequency (KHz)	Practical Frequency (KHz)	Capacitor C in µf	Resistor R_A in KΩ	Resistor R_B in KΩ
1						
2						
3						

Theoretical Calculations:

GRAPH SHEET:



RESULT:

Exercise:

1. Derive the expression of Frequency for the Astable Multivibrator

EXPERIMENT-13

MONOSTABLE MULTIVIBRATOR USING A 555 TIMER

AIM: To use a 555 timer as Monostable Multivibrator

APPARATUS:
IC 555 – 1No.

Resistors – 100kΩ, 47kΩ(2), 470Ω

Capacitors – 10µF, 10nF

Switch (S1)

Analog Discovery Kit

Bread Board

CIRCUIT DIAGRAM:

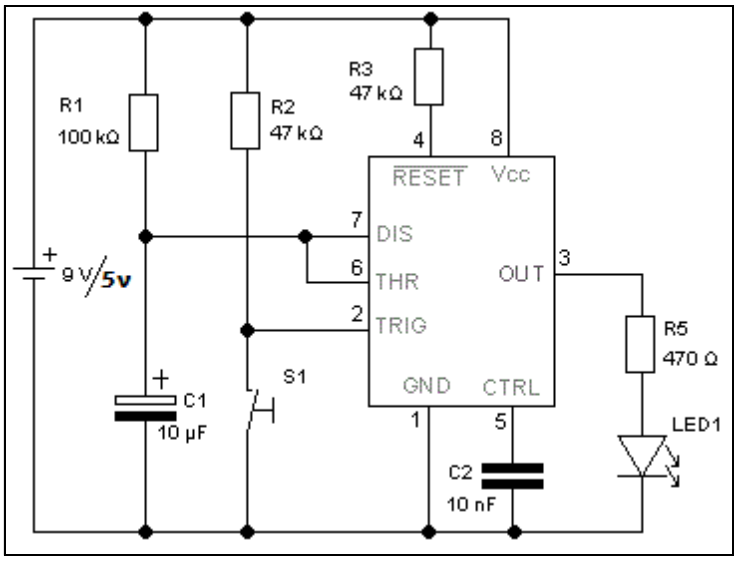


Figure: Monostable Multivibrator

THEORY:

Monostable multivibrator often called a *one shot* multivibrator is a pulse generating circuit in which the duration of this pulse is determined by the RC network connected externally to the 555 timer. In a stable or standby state, the output of the circuit is approximately zero or a logic-low level.

When external trigger pulse is applied output is forced to go high (≈ V_{CC}). The time for which output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until trigger pulse is again applied. Then the cycle repeats. The monostable circuit has only one stable state (*output low*) hence the name *monostable*.

Initially when the circuit is in the stable state i.e , when the output is low, transistor Q1(internal of 555 Timer) is ON and the capacitor C is shorted out to ground. Upon the application of a negative trigger pulse to pin 2, transistor Q1(internal of 555 Timer) is turned OFF, which releases the short circuit across the external capacitor C and drives the output high. The capacitor C now starts charging up towards V_{CC} through R. When the voltage across the capacitor equals 2/3 V_{CC}, comparator 1's output switches from low to high, which inturn drives the output to its low state via the output of the flip-flop.

At the same time the output of the flip-flop turns transistor Q1(internal of 555 Timer) ON and hence the capacitor C rapidly discharges through the transistor. The output of the Monostable remains low until a trigger pulse is again applied. Then the cycle repeats.

The pulse width of the trigger input must be smaller than the expected pulse width of the output waveform. Also the trigger pulse must be a negative going input signal with amplitude larger than 1/3 V_{CC}.

The time during which the output remains high is given by

$$t = 1.1RC \quad \text{seconds}$$

where R is in Ohms and C is in Farads.

Once triggered, the circuit's output will remain in the high state until the set time, *t* elapses. The output will not change its state even if an input trigger is applied again during this time interval *t.* The circuit can be reset during the timing cycle by applying negative pulse to the reset terminal. The output will remain in the low state until a trigger is again applied.

PROCEDURE:

1. Connect the trigger circuit as shown in the circuit diagram.
2. Apply the square wave input to the trigger circuit and apply the output of this trigger circuit to the pin no. 2 of the 555 timer.
3. Now observe the output of the monostable multivibrator and compare the values of the gate width with the theoretical values.
4. The gate width of the monostable multivibrator is given by, GATE WIDTH = 1.1RC.

WAVEFORMS:

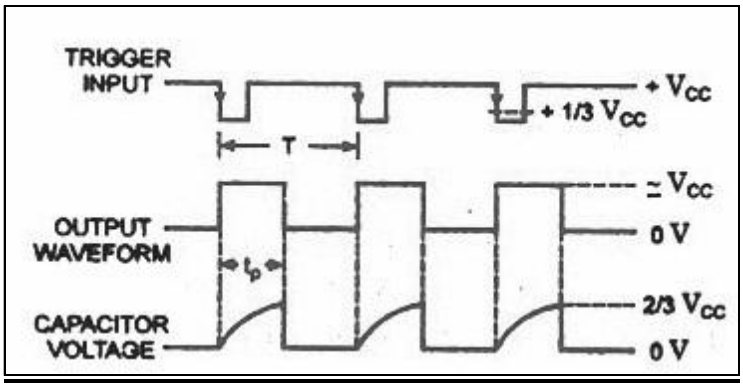


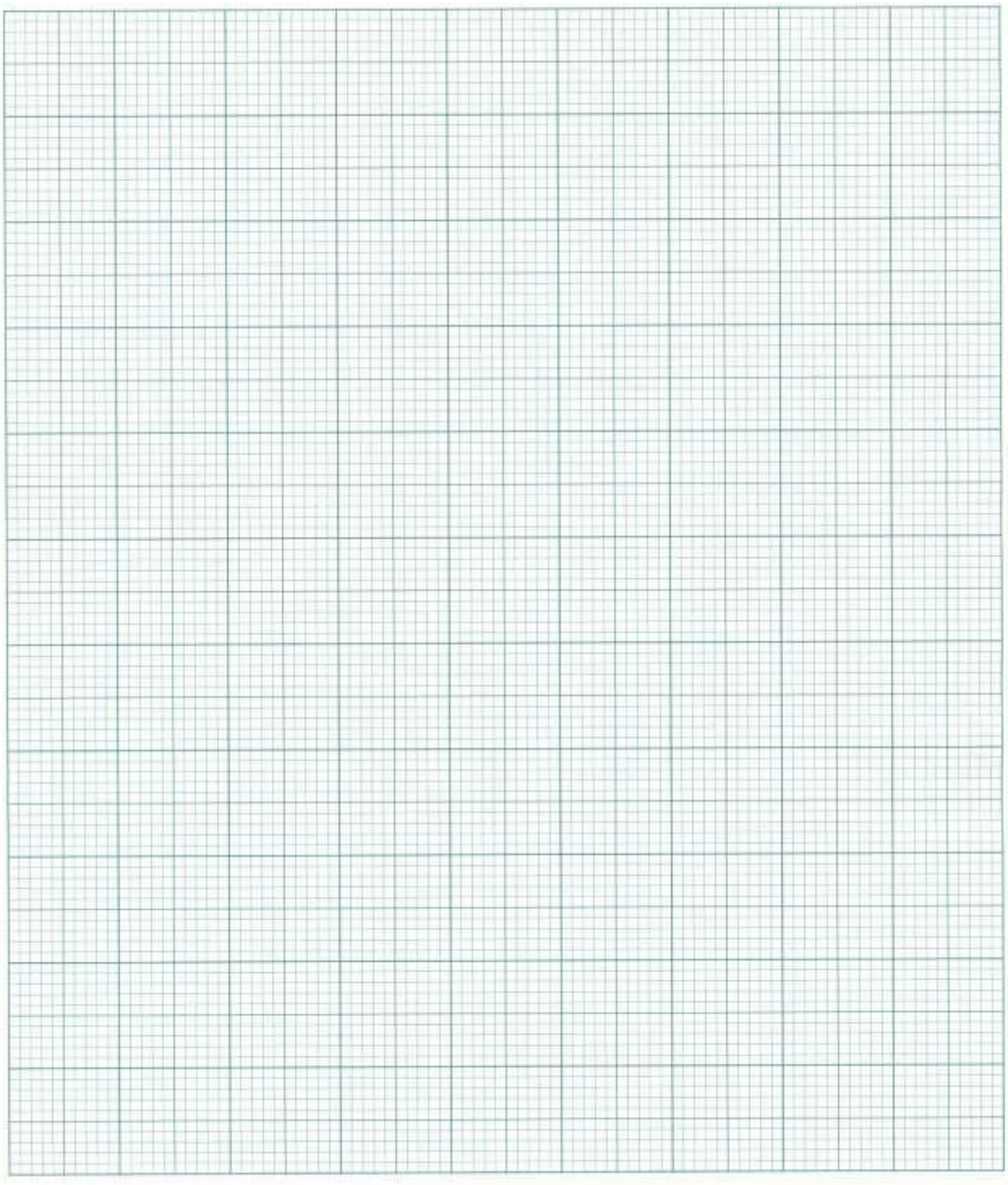
Figure: Model Waveforms

Tabular Column:

S.No.	R (kΩ)	C (µF)	GATE WIDTH OF THE OUPUT	
			THEORITICAL	PRACTICAL

Theoretical Calculations:

GRAPH SHEET:



RESULT:

EXPERIMENT-14
Voltage to Frequency Converter

AIM: To construct and demonstrate Voltage/Frequency and Frequency/Voltage Converter using LM741/OP27.

APPARATUS:
LM741/OP27 or its equivalent and NE 555 Timer IC

Resistors – 5K6 and 2K7 with 0.5% tolerance and 10K potentiometer

Capacitor – 0.01µF and 0.022 µF

Analog discovery Kit (AD Kit)

Bread Board

CIRCUIT DIAGRAM:

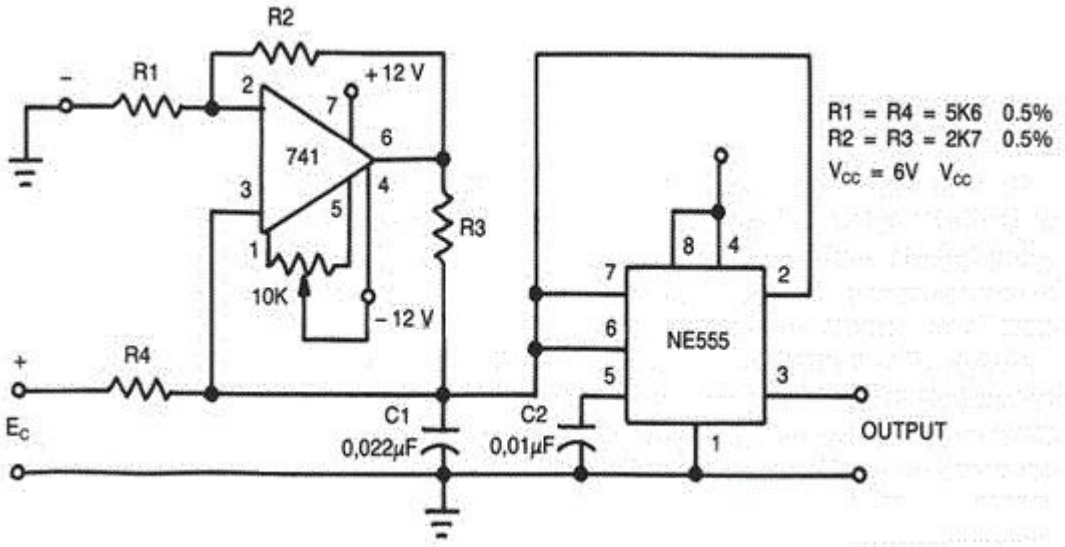


Figure: Voltage to Frequency Converter

THEORY:

Using this circuit, we can accept positive or negative or differential control voltages. When the control voltage is zero, the output frequency is zero. To charge the timing capacitor C1 linearly, the 741 op amp forms a current source controlled by the voltage EC. The capacitor charges and discharges between 1/3 Vcc and 2/3 Vcc because NE555 is connected in the astable mode. 10K potentiometer is adjust the offset so that the frequency is zero when the input is zero. For component values shown f≈4.2 Ec kHz, the output frequency will be proportional to the difference between the two voltages if two dc voltages are applied to the ends of R_1 and R_4.

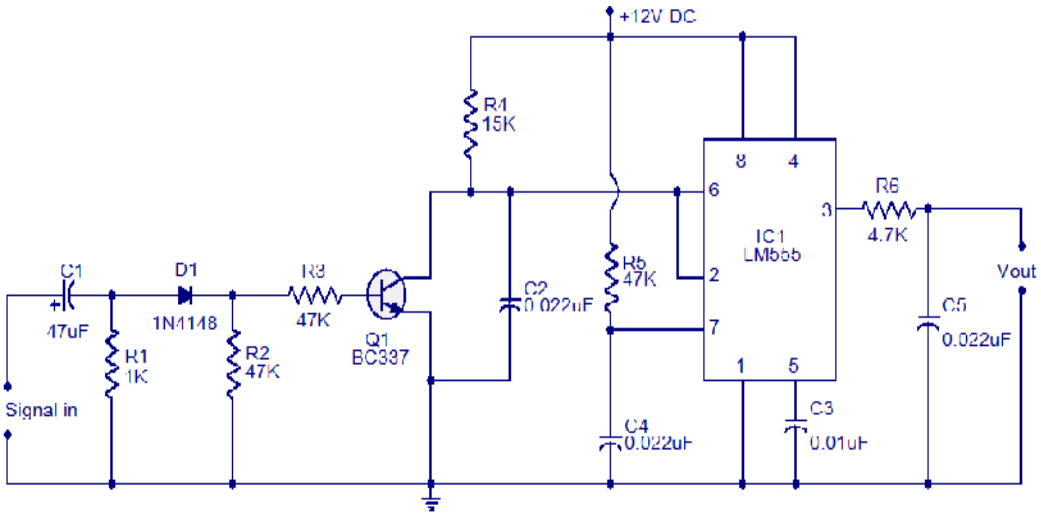
PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Apply the control voltage signal to the circuit.
3. Using 10K potentiometer adjust the offset so that the frequency is zero when the input is zero.
4. Measure the output signal frequency and magnitude using Ad kit scope.
5. Change the value of potentiometer to change the output signal frequency.

EXERCISE:

Design a Frequency to Voltage Converter as shown in the following circuit diagram
And conduct the experiment.

CIRCUIT DIAGRAM:



THEORY:

Such a circuit finds numerous applications in projects like digital frequency meters, tachometers etc. The circuit is mainly based on a LM555 timer IC. The IC is wired in mono shot mode to convert the input frequency into a fixed pulse width, variable frequency PWM signal. Resistors R4 and capacitor C2 provides the necessary timing for the circuit. The transistor T1 forms a discharge path parallel to C2 which is necessary for re triggering the IC. Capacitor C1 acts as an input DC decoupler.

EXPERIMENT-15

LOGICAL GATES

Aim: To write Verilog code for logical AND & OR Gates .

Software tools: Xilinx ISE 9.2i

Verilog Code:

AND GATE:

```
module and(a,b,c);
input a, b;
output c;
assign c=a&b;
endmodule
```

OR GATE:

```
module or(a,b,c);
input a, b;
output c;
assign c=a | b;
endmodule
```

Test Bench:

```
module add_tb_v;
// Inputs reg a; reg b;
// Outputs
wire c;
// Instantiate the Unit Under Test (UUT)
add uut (
.a(a),
.b(b),
.c(c)

);
initial begin
// Initialize Inputs
a = 0;   b = 0;                    // Wait 100 ns for global reset to finish
#100;a=0;b=1;
#100;a=1;b=0;
#100;a=1;b=1;
        end endmodule
```

Truth Table:

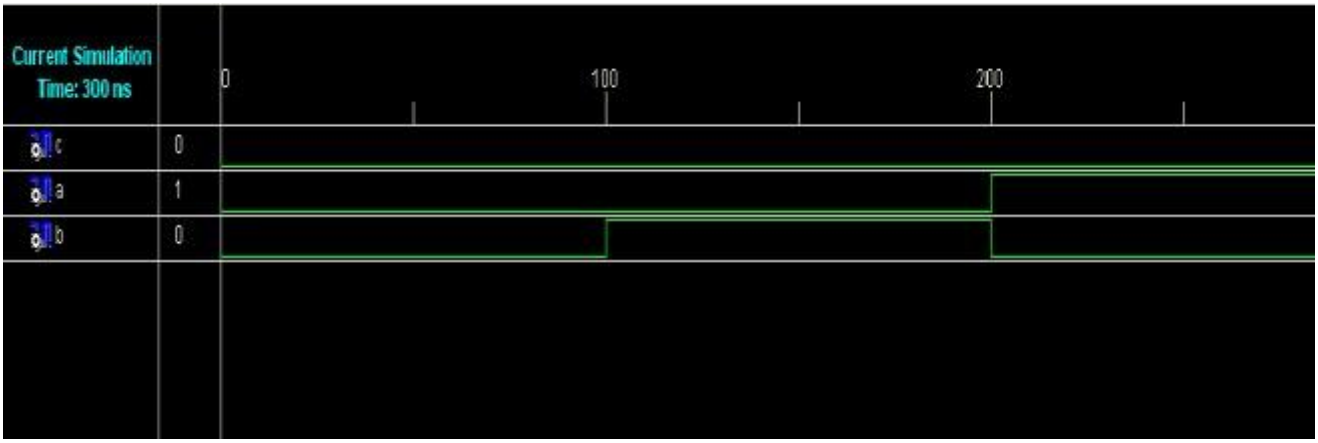
AND Gate:

A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

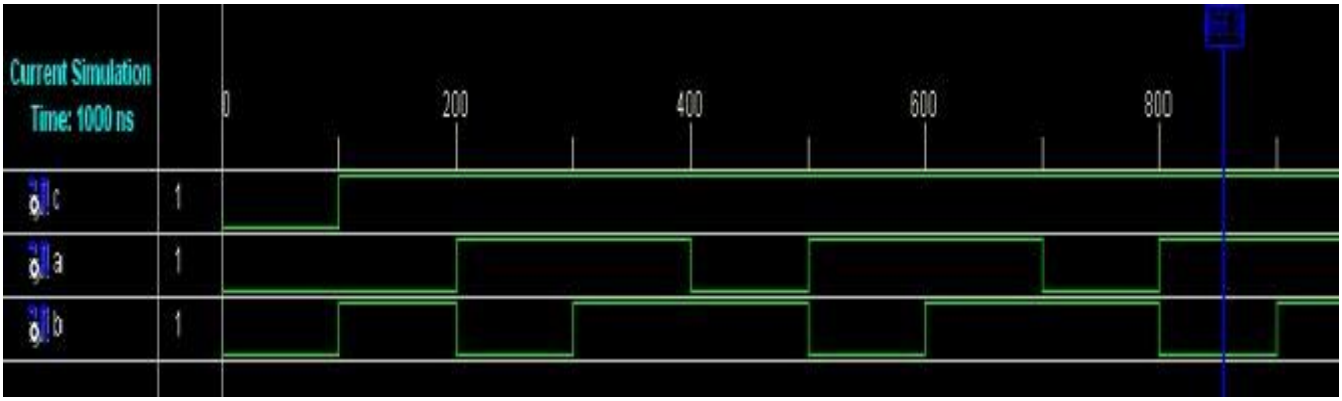
OR Gate:

INPUTS		OUTPUT
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

Simulation Result: AND Gate:



OR Gate:



Exercise: Execute remaining logic gates and write their truth tables with logic gate symbols.

EXPERIMENT-16

HALFADDER

Aim: To write verilog code for half adder and Full adder.

Software tools: Xilinx ISE 9.2i

Verilog Code:

```
module fulladder(a,b,c,sum,carry);
        input a, b, c;
        output sum,
        carry; wire s1,
        c1, c2;
        had
        h1(a,b,s1,c1); had
        h2(s1,c,sum,c2);
        assign
        carry=c1|c2;
endmodule
```

Verilog Code for half adder:

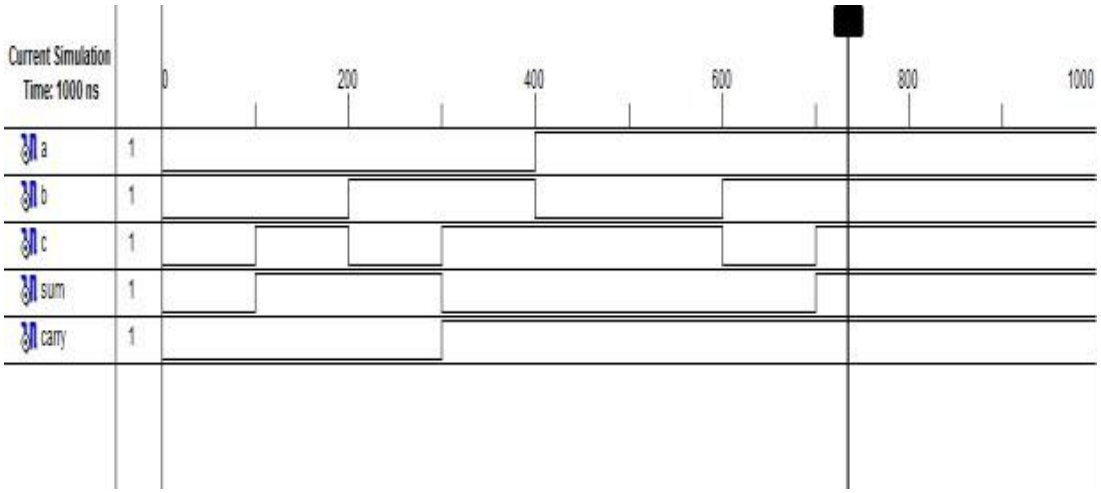
```
module
        had(a,b,s,c
        ); input  a,
        b; output
        s, c; assign
        s=a^b;
        assign
        c=a&b;
endmodule
```

Test Bench:

```
module fulladder_tb_v;
        // Inputs reg a; reg b; reg c;
```

```
// Outputs wire sum; wire carry;
// Instantiate the Unit Under Test (UUT)
fulladder uut (
        .a(a),
        .b(b),
        .c(c),
        .sum(sum),
        .carry(carry)
);
initial begin
        // Initialize Inputs
        a = 0;   b = 0;   c = 0;
        // Wait 100 ns for global reset to finish
        #100;a=0;b=0;c=1;
        #100;a=0;b=1;c=0;
        #100;a=0;b=1;c=1;
        #100;a=1;b=0;c=1;
        #100;a=1;b=0;c=1;
        #100;a=1;b=1;c=0;
        #100;a=1;b=1;c=1;
End
 endmodule
```

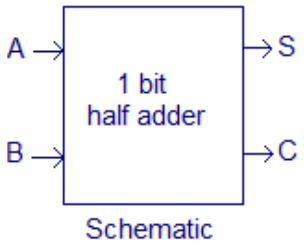
Simulation Result:



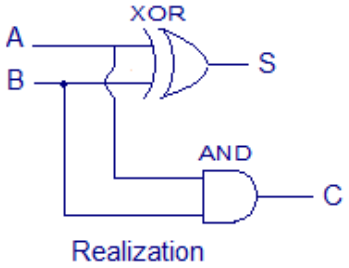
Circuit Diagram:

Inputs		Outputs	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Truth table



Schematic



Realization

Circuit Diagram of Half adder

Exercise:

1. Draw the Circuit diagram and Truth Table for Full Adder.

EXPERIMENT-17

HALF SUBTRACTOR

Aim: To write a verilog code for half subtractor.

Software tools: Xilinx ISE 9.2i

Verilog code:

```
module halfsub(a, c, b, d);
input a; input c; output b; output d;
assign d=a^c;
assign b=((!a)&c);
endmodule
```

Test Bench:

```
module halfsub_tb_v;
reg a; reg c; wire b; wire d;

halfsub uut (

.a(a),

.c(c),

.b(b),

.d(d));

always

begin a =

0;c = 0;

#100;a=0;c=1;

#100;a=1;c=0;

#100;a=1;c=1;
```

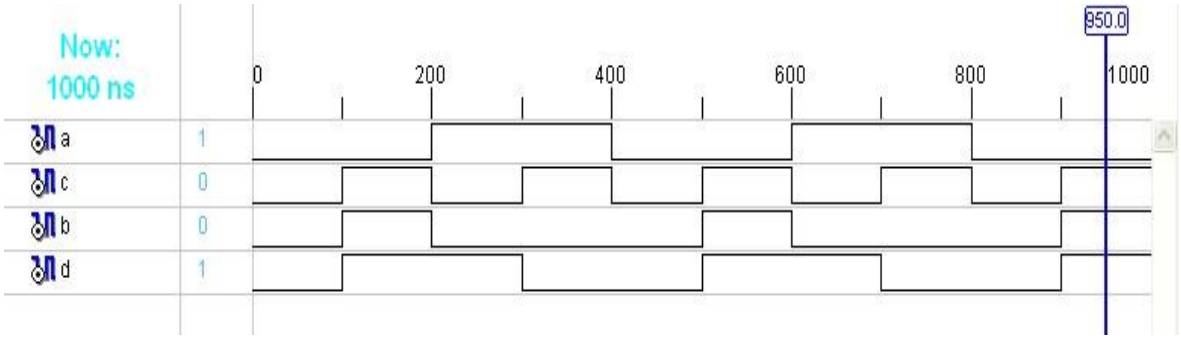
#100;

end

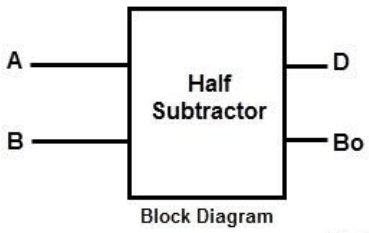
endmo

dule

Simulation Result:



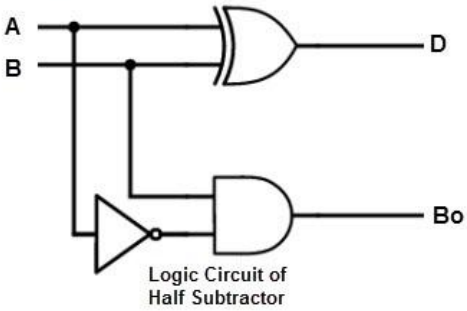
Circuit Diagram:



Block Diagram

A	B	D	B_o
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Truth Table



Logic Circuit of
Half Subtractor

Half Adder Circuit Diagram

EXPERIMENT-18

FULL SUBTRACTOR

Aim: To write a verilog code for full subtractor.

Software tools: Xilinx ISE 9.2i, Quartus II 6.0

Verilog code:

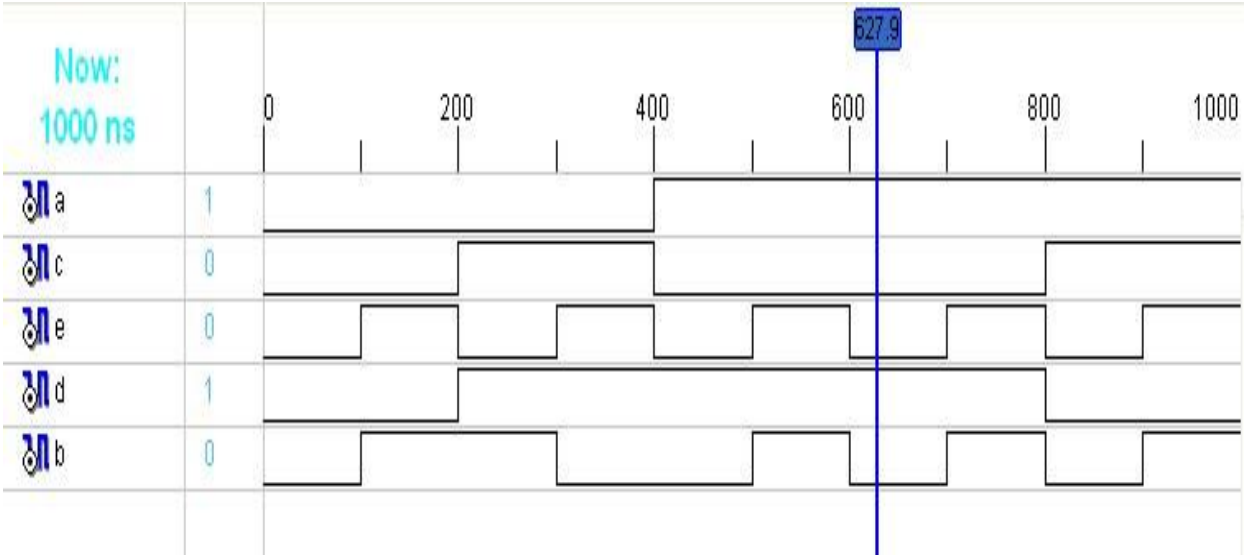
```
module fullsubtractor(a, b, c, d, br);
input a; input b; input c; output d; output br;
assign d=(c+(!c)&(a^b));
assign br=((!a)&b)+c;
endmodule
```

Test Bench:

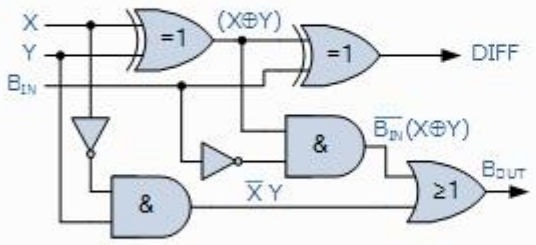
```
module fullsub_tb_v;

reg a; reg c; reg e; wire b; wire d;

fullsub uut (

.a(a),

.c(c),

.e(e),

.b(b),

.d(d)    );

always begin

        a = 0;c = 0;e = 0;

        #100;a=0;c=0;e=1;

        #100;a=0;c=1;e=0;
```

```
        #100;a=0;c=1;e=1;
        #100;a=1;c=0;e=0;
        #100;a=1;c=0;e=1;
        #100;a=1;c=0;e=0;
        #100;a=1;c=0;e=1;
        #100;a=1;c=1;e=0;
        #100;a=1;c=1;e=1;
        #100;
end
endmo
dule
```

Simulation result:



Circuit Diagram:

Symbol	Truth Table				
	B-in	Y	X	Diff.	B-out
	0	0	0	0	0
	0	0	1	1	1
	0	1	0	1	1
	0	1	1	0	1
	1	0	0	1	0
	1	0	1	0	0
	1	1	0	0	0
	1	1	1	1	1

Circuit Diagram and Truth Table for Full subtractor

EXPERIMENT-19

MULTIPLEXER

Aim: To write a verilog code for 16x1 multiplexer using 2x1 multiplexer.

Software tools: Xilinx ISE 9.2i

Verilog code:

```
module  mux16by1(e,i,s,y);
        input  [15:0]i;
        input  [3:0]s;
        input  e;
        output  y;
        wire   [7:0]i1;
        wire   [3:0]i2;
        wire  [1:0]i3;
        mux2by1 m1(e,i[0],i[1],s[0],i1[0]);
        mux2by1  m2(e,i[2],i[3],s[0],i1[1]);
        mux2by1  m3(e,i[4],i[5],s[0],i1[2]);
        mux2by1  m4(e,i[6],i[7],s[0],i1[3]);
        mux2by1  m5(e,i[8],i[9],s[0],i1[4]);
        mux2by1  m6(e,i[10],i[11],s[0],i1[5]);
        mux2by1  m7(e,i[12],i[13],s[0],i1[6]);
        mux2by1  m8(e,i[14],i[15],s[0],i1[7]);
        mux2by1  m9(e,i1[0],i1[1],s[1],i2[0]);
        mux2by1  m10(e,i1[2],i1[3],s[1],i2[1]);
        mux2by1  m11(e,i1[4],i1[5],s[1],i2[2]);
        mux2by1  m12(e,i1[6],i1[7],s[1],i2[3]);
        mux2by1  m13(e,i2[0],i2[1],s[2],i3[0]);
```

```
        mux2by1  m14(e,i2[2],i2[3],s[2],i3[1]);
        mux2by1  m15(e,i3[0],i3[1],s[3],y);
endmodule
```

Verilog code for 2x1mux:

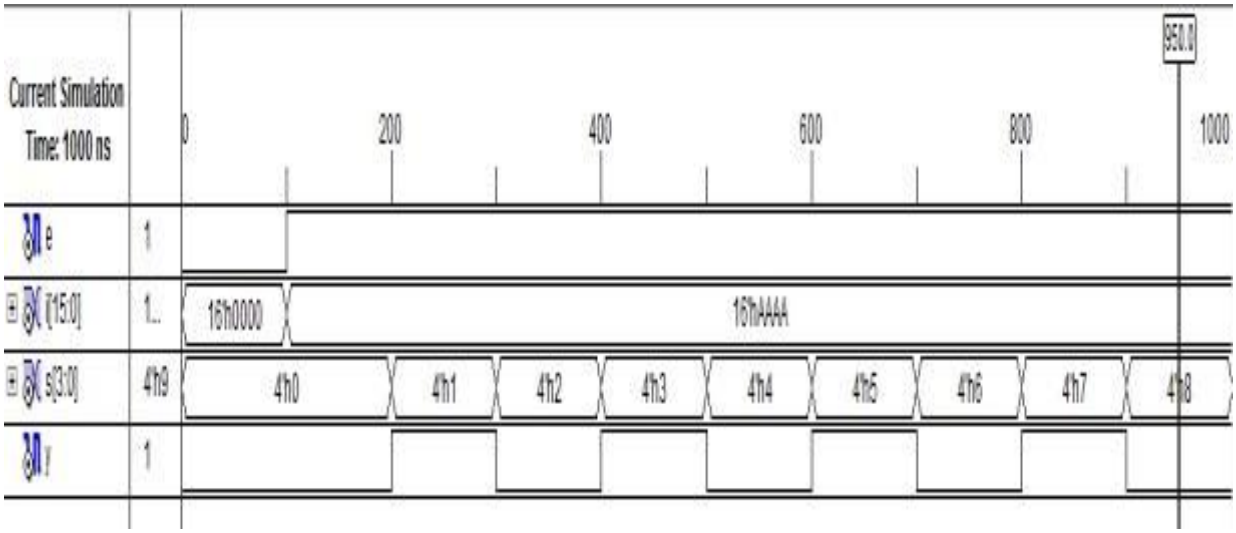
```
module mux2by1(e,a,b,s,y);
        input  s,  e;
        input  a,  b;
        output y;
        assign y=(e&~s&a)|(e&s&b);
endmodule
```

Test Bench:

```
module mux16by1_tb_v;

        // Inputs
        reg e;
        reg [15:0] i;
        reg [3:0] s;

        // Outputs
        wire y;

        // Instantiate the Unit Under Test (UUT)
        mux16by1 uut (
                .e(e),
                .i(i),
                .s(s),
                .y(y)
```

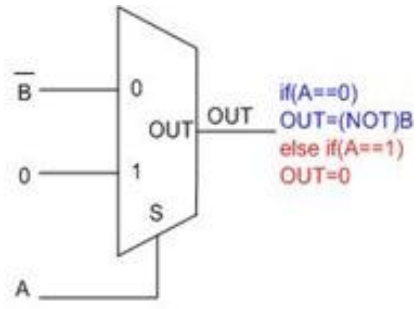
```
	);

	initial begin
		// Initialize Inputs
		e = 0;
		i = 0;
		s = 0;

		// Wait 100 ns for global reset to finish
		#100;e=1;i=16'haaaa;s=4'h0;
		#100;s=4'h1;
		#100;s=4'h2;
		#100;s=4'h3;
		#100;s=4'h4;
		#100;s=4'h5;
		#100;s=4'h6;
		#100;s=4'h7;
		#100;s=4'h8;
		#100;s=4'h9;
		#100;s=4'ha;
		#100;s=4'hb;
		#100;s=4'hc;
		#100;s=4'hd;
		#100;s=4'he;
		#100;s=4'hf;

	end

endmodule
```

Simulation Result:



Circuit Diagram:

Inputs		Output
A	B	OUT
0	0	1
0	1	0
1	0	0
1	1	0



Circuit diagram of 2x1 Multiplexer

EXPERIMENT-20
2x4 DECODER

Aim: To write a verilog code for 2x1 decoder.

Software tools: Xilinx ISE 9.2i

Verilog code:

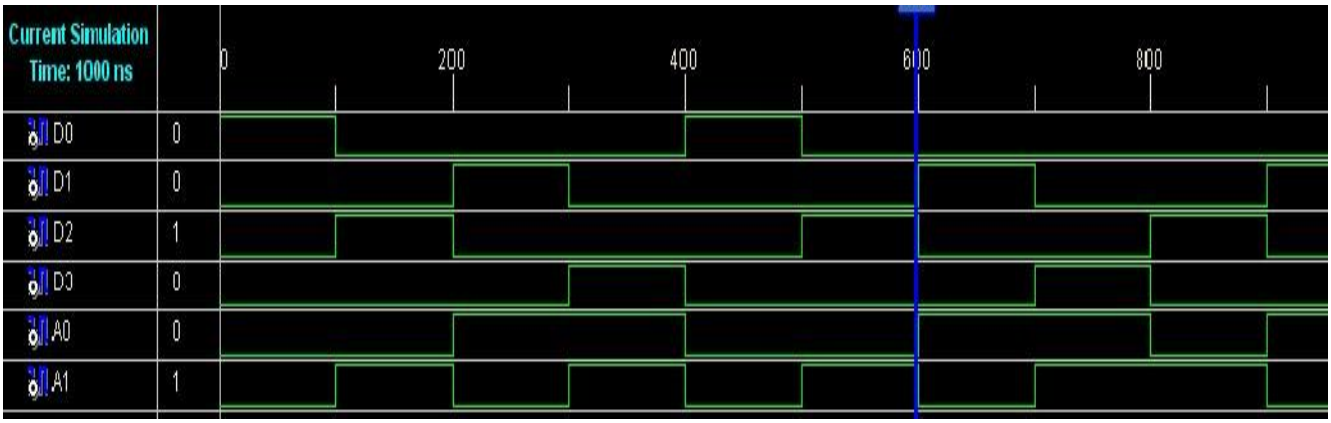
```
module decoder(A0,A1,D0,D1,D2,D3);
input A0,A1;
output D0,D1,D2,D3;
assign D0=!A0&!A1;
assign D1=A0&!A1;
assign D2=!A0&A1;
assign D3=A0&A1;
endmodule
```

Test Bench:

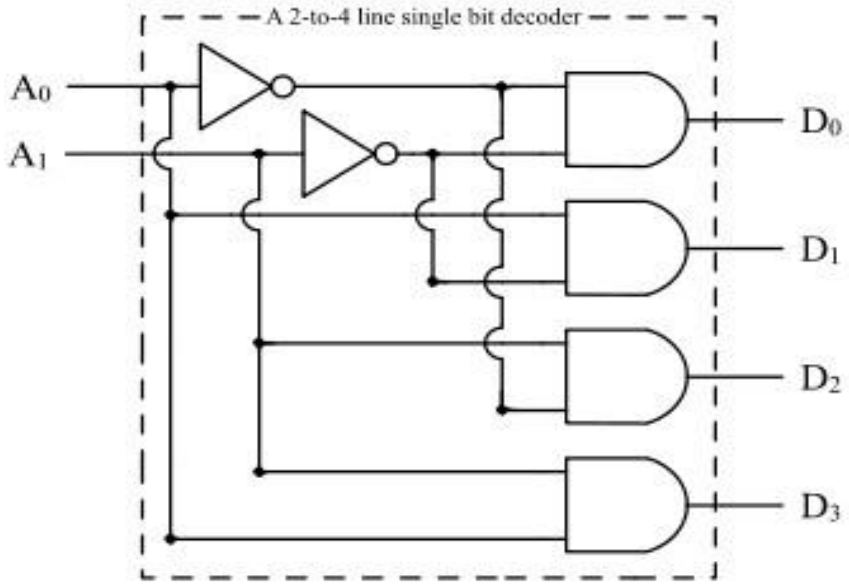
```
module decode_tb_v;

    // Inputs
    reg A0;
    reg A1;

    // Outputs
    wire D0;
    wire D1;
    wire D2;
    wire D3;

    // Instantiate the Unit Under Test (UUT)
```

```
	decoder uut (
		.A0(A0),
		.A1(A1),
		.D0(D0),
		.D1(D1),
		.D2(D2),
		.D3(D3)
	);

	initial begin
		// Initialize Inputs
		A0 = 0;
		A1 = 0;

		// Wait 100 ns for global reset to finish
		#100;A0 = 0;A1 = 1;
		#100;A0 = 1;A1 = 0;
		#100;A0 = 1;A1 = 1;
		#100;A0 = 0;A1 = 0;
		#100;A0 = 0;A1 = 1;
		#100;A0 = 1;A1 = 0;
		#100;A0 = 1;A1 = 1;
		#100;A0 = 0;A1 = 1;
		#100;A0 = 1;A1 = 0;
		#100;A0 = 1;A1 = 1;

		// Add stimulus here

	end

endmodule
```

Simulation Result:



Circuit diagram:



Truth Table:

A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

EXPERIMENT-21
D-FLIP FLOP

Aim: To write a verilog code for D-flip flop.
Software tools: Xilinx ISE 9.2i
Verilog code:

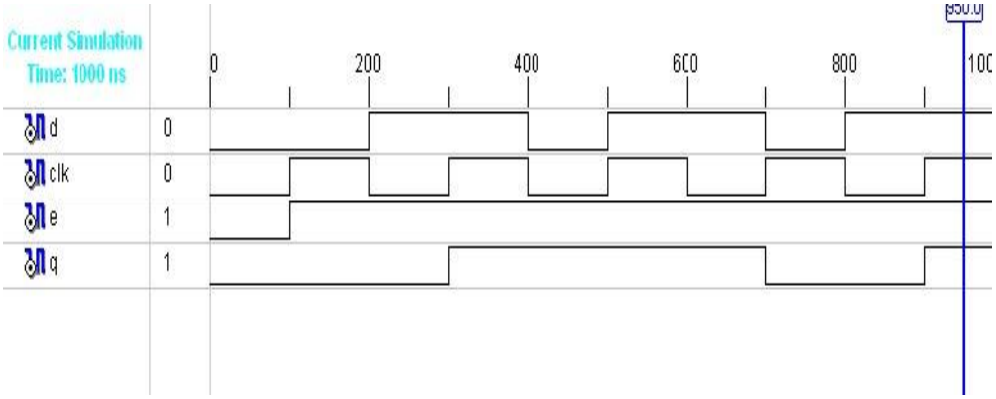
```
module dflipflop(clk, e, d, q);
input clk;
input e; input
d;
output reg q;
always@(posedge clk or negedge e)
q=d;
endmodule
```

Test bench:

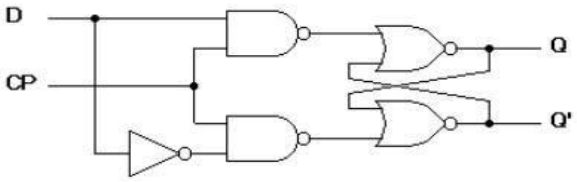
```
module dflipflop_tb_v;
// Inputs reg clk;
reg e; reg d;
// Outputs wire q;
// Instantiate the Unit Under Test (UUT)
dflipflop uut (
.clk(clk),
.e(e),
.d(d),
.q(q)
);
initial begin
// Initialize Inputs clk = 0;
e = 0;
d = 0;
```

```
end
// Wait 100 ns for global reset to finish always#100 clk=~clk;
always begin
//Add stimuls here
#100;e=1;d=0;

#100;d=1;

#100;

end

endmodule
```

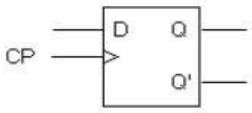
Simulation result:



Circuit Diagram:



(a) Logic diagram with NAND gates



(b) Graphical symbol

Q D	Q(t+1)
0 0	0
0 1	1
1 0	0
1 1	1

(c) Transition table

Clocked D flip-flop

Circuit Diagram for D flip Flop

EXPERIMENT-20
T-FLIP FLOP

Aim: To write a verilog code for T-flip flop.

Software tools: Xilinx ISE 9.2i

Verilog code:

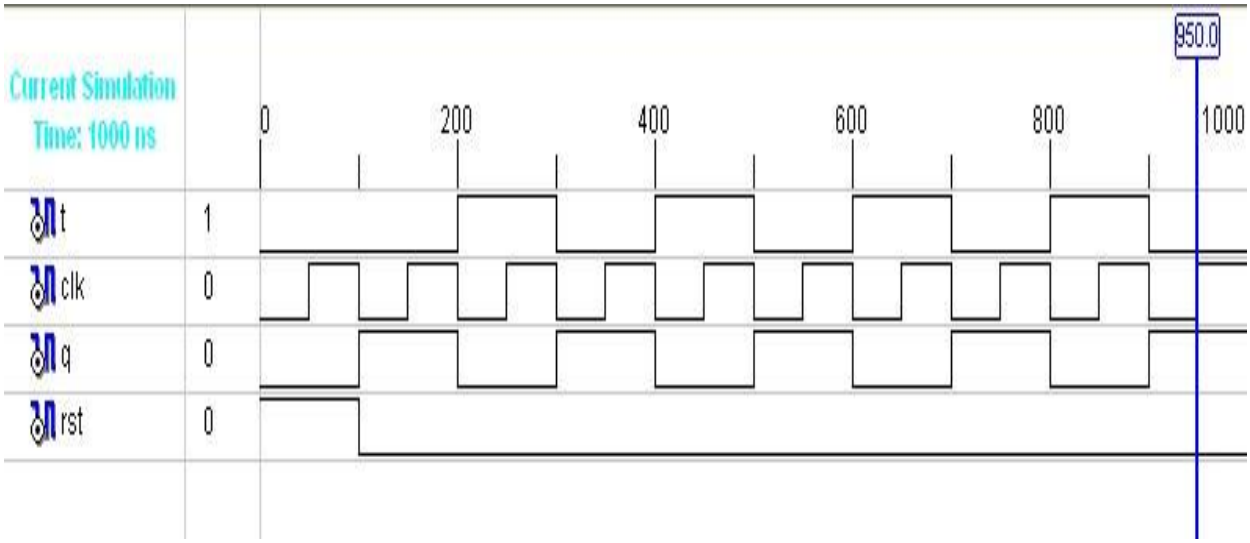
```
module t_ff(t, clk, rst, q);
input t; input
clk; input rst;
output reg q;
always @ (posedge rst or negedge clk)
begin if(rst)
q=1'b0;
else q=~t;

end
endmodule
```

Test bench:

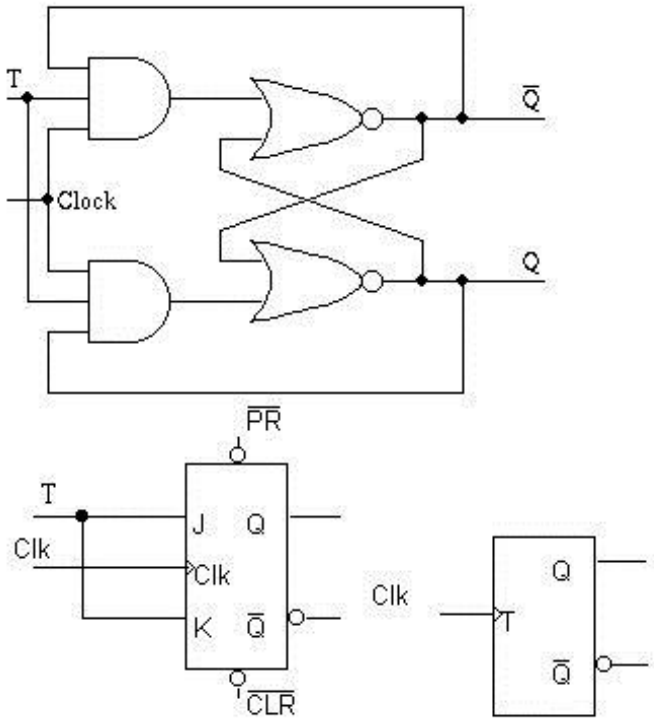
```
module t_ff_tb_v;

// Inputs reg t;

reg clk;

reg rst;

// Outputs wire q;

// Instantiate the Unit Under Test (UUT)

t_ff uut (

.t(t),

.clk(clk),

.rst(rst),
```

```
.q(q)

);
initial begin
        // Initialize Inputs clk = 0;
rst = 1;
t=0;

// Wait 100 ns for global reset to finish

#100; rst=0;

end

always #50 clk=~clk;
always begin
#100; t=0;
#100; t=1;
// Add stimulus here
end endmodule
```

Simulation waveform:



Circuit Diagram:



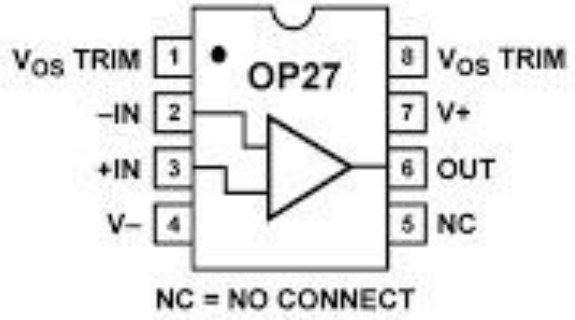
T-Flip Flop Circuit Diagram

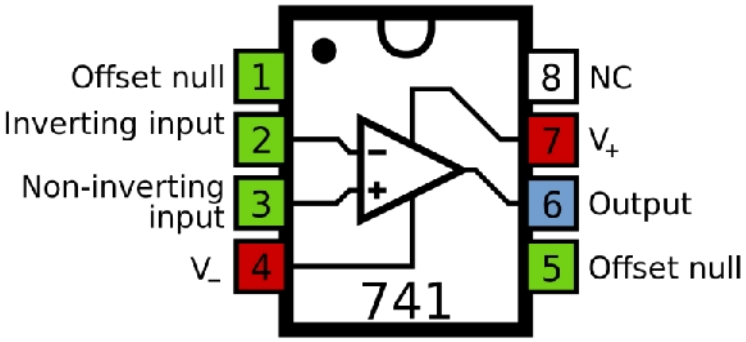
Exercise:

1. Draw the Truth Table for T-Flip Flop
2. Write the Verilog program for J-K Flip Flop.

Annexure

1. **Pin Configuration of Operational Amplifier OP27**





2. **Pin Configuration of Operational Amplifier LM324**

Pin configuration of 555 Timer